TEKTRONIX®

P7001
READOUT INTERFACE
(670-2385-00)

INSTRUCTION MANUAL

Tektronix, Inc.
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Serial Number _____

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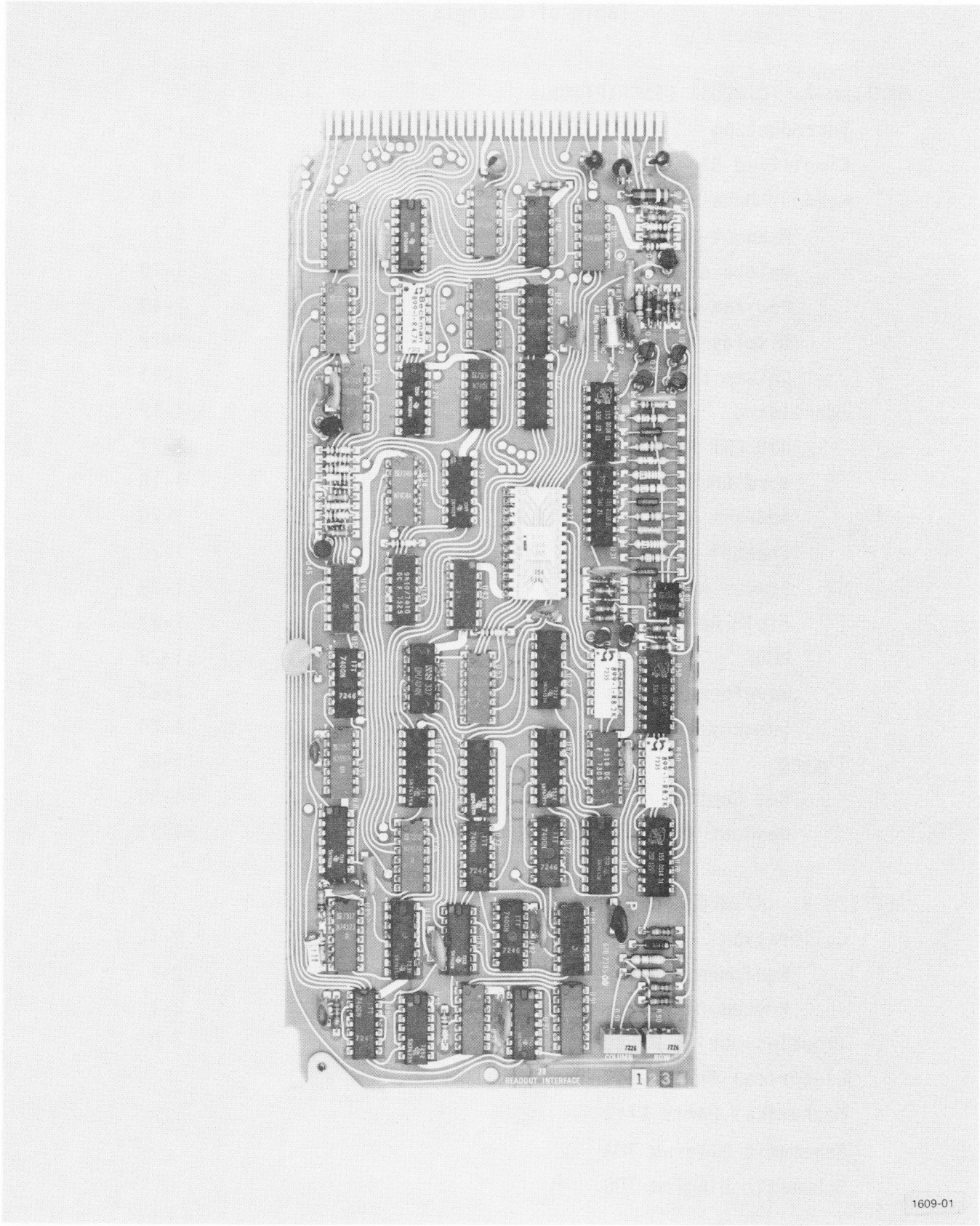

P7001 Readout Interface Card.

SECTION 1

CIRCUIT DESCRIPTION

Introduction

An understanding of the 7000 Series Readout System is a prerequisite for understanding the operation of the P7001 Readout Interface Card. Refer to the 7704A Service Manual for a detailed description of the 7000 Series Readout.

The Readout Interface Card has 11 dedicated pins with the signals shown in Fig. 1-1. The Readout Interface Card plugs into the P7001

Dedicated Pin	Signal Command	Application
B1	READOUT INTENSITY	Disables Readout Interface Card when Display Unit readout intensity control is off except during STORE mode.
A27 A28 B28	CH ADD 2 CH ADD 1 CH ADD 4	Channel location information from Acquistion Unit readout board.
B29	PLUG-INS	TTL level signal from Front Panel/ Z-Axis card. Low when Display Source is Plug-ins.
A33	READOUT TRIGGER	Timing trigger from Acquisition Unit readout board.
A35	PLUG-IN READOUT DISABLE	When low, turns off readout information from the Plug-ins.
A36	DISPLAY SKIP	From Acquisition Unit readout board. Used to skip display for a given "timeslot".
B33 B35	COLUMN DATA ROW DATA	Sends information to Acquisition Unit readout board during read from Memory. Receives information from Acquisition Unit plug-ins during STORE mode.
B34	ROW & COL COM (B33 and B35 shield, raised to +15 V)	Common shield tie point. Used to carry +15 V reference from Acquisition Unit readout board.

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Fig. 1-1. Readout Interface dedicated pins.

Main Interface Board, connector J5 (see the Main Interface Manual 070-1604-00). This board contains the P7001 Asynchronous Bus; consisting of Control, Address, Data, and Power lines for each of the cards plugged into it. There are also dedicated pins for use by individual cards requiring special signals.

An overview of the Digital Processing Oscilloscope (DPO), showing the P7001 Readout Interface Card in relation to the rest of the DPO, is shown in Fig. 1-2. Note that there are two Readout devices. One is in the P7001, called the Readout Interface Card. The other is in the A7704 Acquisition Unit, called the Readout Board.

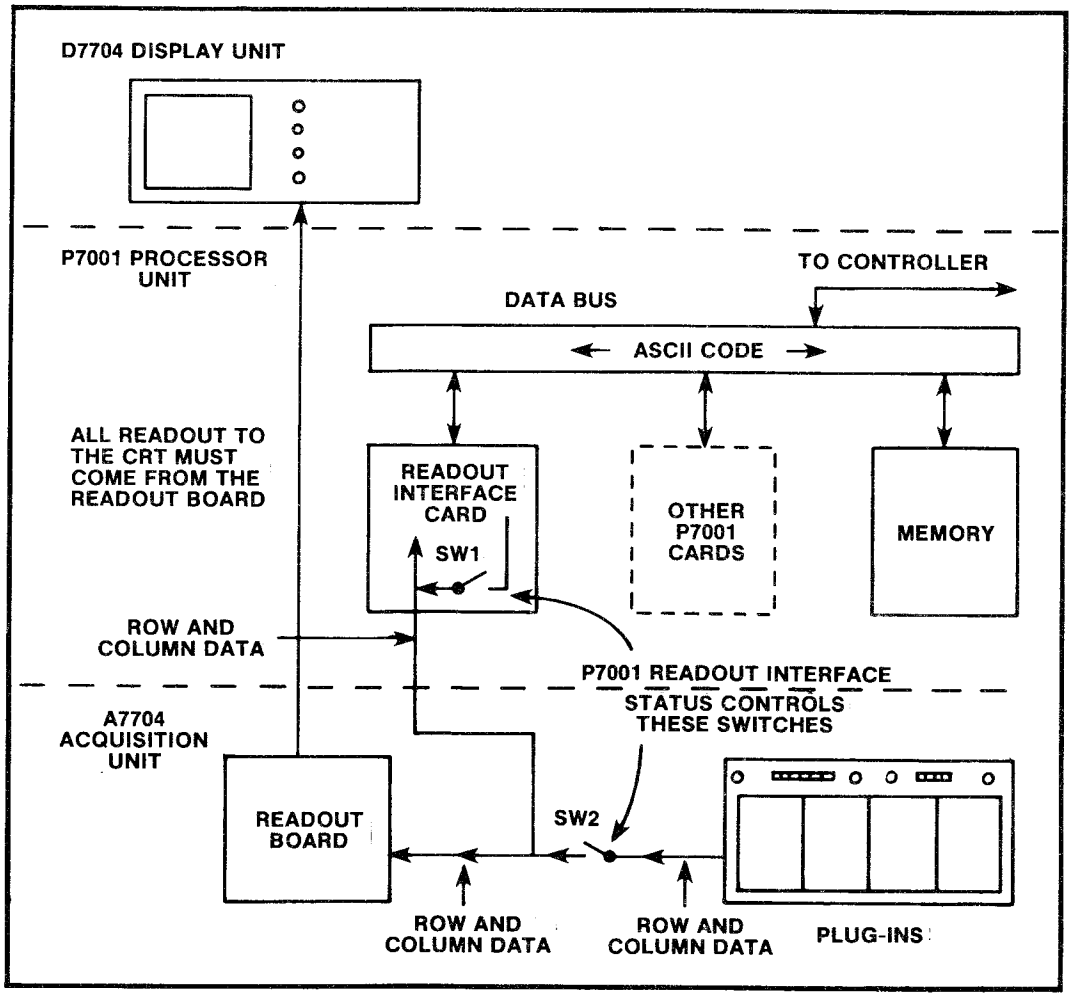

Fig. 1-2. Readout overview.

The switches shown in Fig. 1-2 are hypothetical and are controlled by the Status of the Readout Interface Card. They are actually transistor circuits. The "switches" indicate the selection of readout information to be displayed on the CRT. "Switch" 1 is open when storing information in Memory and closed when reading from Memory. "Switch" 2 is controlled by PLUG-IN READOUT DISABLE (Diag. 10A) and is open during display of readout information from Memory and closed at all other times.

Fig. 1-3 illustrates the selection of readout information that is to be displayed on the CRT. For example, if the DISPLAY SOURCE is MEMORY and the Readout Interface's DATA HANDLING mode is HOLD then the source of the readout information being displayed on the CRT is from Memory. If the DISPLAY SOURCE is changed to PLUG-INS then the source of the readout information being displayed on the CRT is from the Plug-ins.

READOUT SOURCE		DATA HANDLING MODE: STORE	HOLD
DISPLAY SOURCE:	PLUG-INS	PLUG-INS	PLUG-INS
	BOTH	PLUG-INS	MEMORY
	MEMORY	PLUG-INS	MEMORY

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Fig. 1-3. Readout source.

During STORE mode, all readout information being displayed on the CRT comes directly from the Plug-ins. The Readout Interface Card just monitors that information, converts it to ASCII code, and stores it in Memory.

Simplified Block Diagram of Readout Data Path

The simplified block diagram, Fig. 1-4, shows a general routing of the readout information. The STORE input to the ROM (Read only Memory) is LOW during HOLD and HIGH during STORE. The HOLD mode of the P7001 sets the Readout Interface Card to display information from Memory (if the DISPLAY SOURCE is BOTH or MEMORY). This signal path is from the P7001 Data Bus to the ROM Input Selector as ASCII data. This data is then sent to the ROM Input Latch and latched when the STROBE signal is received from the Readout Controller (Diag. 10B).

The ROM is used for two different conversions, one during STORE and one during HOLD. The most significant address bit is controlled by the "STORE" status which selects one of two groups of 128 address combinations of the 256 X 8 ROM. During STORE, seven (of eight) address lines to the ROM contain row and column information. During HOLD, the seven (of eight) address lines to the ROM contain ASCII data.

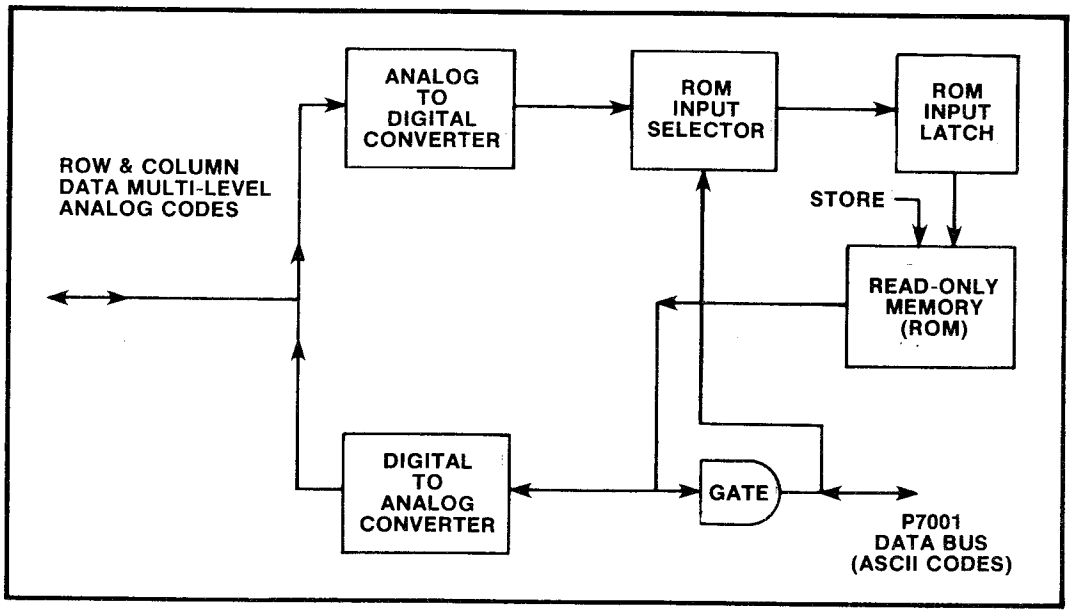


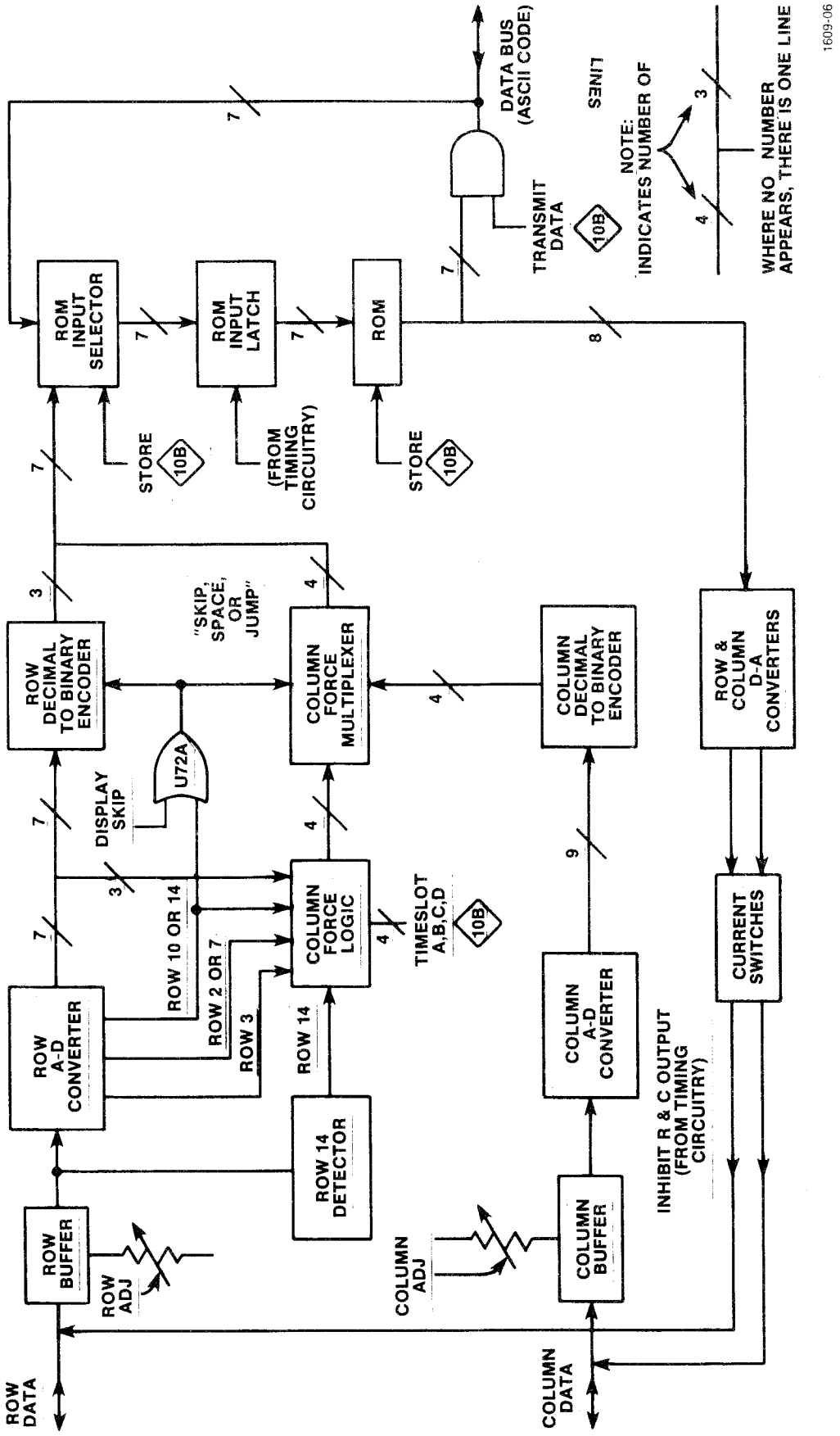
Fig. 1-4. Simplified block diagram of readout data path.

During HOLD the output of the ROM is digital data, which is then converted to row and column analog current steps by the Digital-to-Analog converters. These analog currents then go to the Acquisition Unit Readout Board for conversion to characters to be displayed on the CRT.

If the Readout Interface Card status is changed to STORE, the Readout Interface Card switches the STORE input to the ROM Input Selector to a HIGH. The ROM Input Selector sends digital row and column information from the A-D Converter to the ROM Input Latch. After the proper timing pulse, that data is clocked into the ROM. The ROM, with STORE HIGH (MSB address, input bit 8), converts the row and column digital data into an ASCII code. This ASCII code is then gated onto the Data Bus, when TRANSMIT DATA is received from the Bus Controller (Diag. 10B); from there it goes to the Memory for storage.

Readout Data Handling

Compare the block diagram in Fig. 1-5 to diagram 10A. Diagram 10A has been marked and labeled to show the circuit components which make up the blocks in Fig. 1-5. For example, the row A-D Converter is U50; the column A-D Converter is U70.


ROW DATA
COLUMN DATA
ROW BUFFER
ROW ADJ
COLUMN ADJ
COLUMN BUFFER
ROW A-D CONVERTER
ROW 14 DETECTOR
COLUMN A-D CONVERTER
ROW 10 OR 14
ROW 2 OR 7
ROW 3
ROW 14
COLUMN FORCE LOGIC
TIMESLOT A,B,C,D
10B
DISPLAY SKIP
U72A
"SKIP, SPACE, OR JUMP"
ROW DECIMAL TO BINARY ENCODER
COLUMN FORCE MULTIPLEXER
COLUMN DECIMAL TO BINARY ENCODER
ROW & COLUMN D-A CONVERTERS
CURRENT SWITCHES
INHIBIT R & C OUTPUT (FROM TIMING CIRCUITRY)
ROM INPUT SELECTOR
ROM INPUT LATCH
ROM
STORE
10B
(FROM TIMING CIRCUITRY)
STORE
10B
TRANSMIT DATA
10B
DATA BUS (ASCII CODE)
NOTE: INDICATES NUMBER OF LINES
WHERE NO NUMBER APPEARS, THERE IS ONE LINE
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Readout Matrix. The Readout Interface converts row and column information to ASCII data that can be stored in the P7001 Memory. Figure 1-6 is a matrix which shows which ASCII character is used for row and column information or operational addresses.

Some 7000 series readout characters have no ASCII code assigned. Therefore, normal ASCII characters have been chosen to provide an equivalent code for storage. The diagonal line, in nine of the blocks, indicate the ASCII substitution of the original 7000 series readout character (Fig. 1-6a). For example: The 7000 series readout character "Ω" - omega, has no ASCII code, so we store the equivalent code "@". The "Ω" will be sent by the Plug-ins, but an ASCII code for the "@" will be stored in Memory. If an "@" is stored in memory by an external controller, it will be displayed on the DPO CRT as "Ω".

Table 1-1 lists the ASCII characters used for the timeslot-dependent operational addresses: SKIP, ZEROS LOGIC, IDENTIFY, and JUMP COMMAND. If a Plug-in sends Row 1, Column 0, in timeslot 1, 2, or 3, then the Readout Interface Card will generate an ASCII "space". For Row 1, Column Ø in timeslot 4 or higher, an ASCII "DELETE" will be generated. IDENTIFY command (Row 3, Column 10 in timeslot 1) causes the Readout Interface card to generate any one of four ASCII characters in timeslot 1, and causes the Readout to produce the message "IDENTIFY" in timeslots 2 through 9 followed by "skip" in timeslot 10, all of which are converted to ASCII by the Readout Interface Card. The operational address portions of the Matrix are referenced to Table 1-1 by: ①, ②, ③, and ④.

ROW NUMBER	CURRENT STEPS (ma)	C-0	C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8	C-9	C-10
	COLUMN NUMBER		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	≥1.0
R-1	0		0	1	2	3	4	5	6	7	8	9
R-2	0.1		↓ / !	<	I	/	+	–	+	C	△ / =	>
R-3	0.2		SEE TABLE 1-1 ① & ②				INVALID READOUT CODES					See TABLE 1-1 ③
R-4	0.3		m	μ / u	n	p	x	K	M	G	T	R
R-5	0.4		S	V	A	W	H	d	B	c	Ω / @	E
R-6	0.5		U	N	L	Z	Y	P	F	J	Q	D
R-7	0.6				DECIMAL POINT 3 / $	DP4 / %	DP5 / &	DP6 / '	DP7 / (			
R-8	0.7											
R-9	0.8						INVALID READOUT CODES					
R-10	0.9	SPACE										
R-14	≥1.3		SEE TABLE 1-1 ④									

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Fig. 1-6. Readout Character Matrix.

	INPUT CODE		ASCII CHAR STORED IN TIMESLOT 1	2	3	4	5	6	7	8	9	10
①	SKIPS:	R1, 4-6, 8, 9/CØ	SPACE									
		R2, 7/CØ	;	SPACE	←			DELETE				→
		R3/CØ	:	SPACE								
②	ZEROS LOGIC: R3/C1 thru 4		:									
③	IDENTIFY: R3/C10		;:]	←				ILLEGAL INPUT				→
④	JUMP COMMAND: R14/CØ-10		?									

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Table 1-1. Characters stored for time-slot dependent operational addresses.

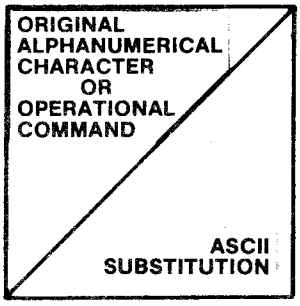

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Fig. 1-6a. P7001 ASCII Substitutions.

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Fig. 1-7 summarizes the readout characters normally used in P7001 Memory, notes the differences between ASCII and 7000 Series characters, and includes the ASCII number for the ASCII code.

ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY
040	SPACE	067	7	107	G	124	T
041(!)*	↓	070	8	110	H	125	U
053	+	071	9	111	I	126	V
055	–	074	<	112	J	127	W
056	.	075(=)*	△	113	K	130	X
057	/	076	>	114	L	131	Y
060	0	100(@)*	Ω	115	M	132	Z
061	1	101	A	116	N	143	c
062	2	102	B	117	O	144	d
063	3	103	C	120	P	155	m
064	4	104	D	121	Q	156	n
065	5	105	E	122	R	160	p
066	6	106	F	123	S	165(u)*	μ

*ASCII character is different from displayed character.

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Fig. 1-7. Readout characters normally used in P7001 Memory.

ASCII		Notes
OCTAL CODE	Char.[2]	(Refer to 7704A Manual for details)
044	$	Decimal placed after 3rd "non-DEL" character in this channel.
045	%	Decimal placed after 4th "non-DEL" character in this channel.
046	&	Decimal placed after 5th "non-DEL" character in this channel.
047	'	Decimal placed after 6th "non-DEL" character in this channel.
050	(	Decimal placed after 7th "non-DEL" character in this channel.
072	:	Indicates a "Scale factor" channel.[3]
073	;	Indicates a "Digital" channel.[3] A "Digital" type channel is indicated if the first ASCII character in the channel is any of the following: !;</+–=>$%&'(
077	?	This channel is not displayed (ignore).[3]
137	_	Do not leave a space; wait for next character or next channel.
177	DEL	Do not leave a space; wait for next character or next channel.

[2]These ASCII characters are not displayed on the CRT.
[3]The following ASCII characters are used only as the first character in a channel: : ; ?

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Fig. 1-8. Operational addresses generated by plug-ins.

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Fig. 1-8 summarizes the additional ASCII characters (with octal equivalents) stored in the P7001 Memory for operational addresses.

DELETE or Underline Option. Operational addresses from the Plug-ins cause the P7001 Readout Interface Card to store the DELETE ASCII character in memory. If a different external device (such as a different computer) is being used to communicate with the P7001, the line from pin 6 to pin 8 of U13 (Diag. 10A) may be removed. This will change the DELETE character to the "Underline" (uppercase 0) character. Figure 1-8 shows octal codes 137, for underline, and 177, for delete, either of which will accomplish the same function.

Row and Column Data. Operational Amplifiers (U40A and U40B) were added to prevent loading the Row and Column current lines. In reality, there is a transfer of voltage steps in proportion to the current steps generated by the Plug-ins. To simplify the description, we will refer to current steps when mentioning the transfer of row and column information between the Readout Interface and the Acquisition Unit Readout Board.

The row analog information (0.1 milliamp current steps) comes into the card at pin B35 (Diag. 10A). The column analog information comes in at pin B33. These are coaxial inputs with their shields tied to pin B34 which is raised to +15V by the Acquisition Unit. This row and column common (+15V) is used as a reference by the A-D Converters (U50 and U70) to insure that the row and column signals are accurately transferred from the Acquisition Unit Readout Board.

U50 and U70 convert the analog information into decimal infor-

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mation presented as "1 of 10" active low output lines. For example, if 0.3 milliamps of row current is sent by the Plug-ins, there would be a LO output at pin 5 of U50 -- designating Row 4 (see Fig. 1-6). This decimal information (active low) is converted by U61 to a binary (one's) complement form. When the P7001 is in the STORE mode, U52 (part of the ROM input selector) would pass the binary complement of the row number to the ROM Input Latch (U54B and U53), where it is stored as part of the address for the ROM.

If the column current from the Acquisition Unit is 0.2 milliamps, the output at pin 6 of U70 would be a LO, designating column 2 from the Plug-ins (see Fig. 1-6). This LO is fed to U71 where it is converted to a binary complement of the "column-1" number. The output of pin 9, U71, is LO, the other output pins are HI.

U62, the Column Force Multiplexer, selects between the output of the Column Decimal to Binary Converter (U71) and the output of the Column Force Logic circuits. Since we are going to be encoding a character and not skip, space, or jump, the Column Force Multiplexer will pass the $\overline{\text{Column - 1}}$ number to the ROM Input Selector. With the P7001 in the STORE mode, our binary number passes to the ROM Input Latch along with the $\overline{\text{ROW}}$ number that we previously stored here.

We now have row and column information at the input to the ROM. With the P7001 still in the STORE mode, the ROM will convert this binary number combination into an ASCII code. Fig. 1-6, the Readout Character Matrix, shows what this character is. Row 4, column 2 is the Greek letter mu (μ). Since there is no ASCII code for μ we

substitute lower case u. The ROM generates 1110101 which is lower case u in ASCII code. This ASCII code is sent to the set of "NAND" gates where it will be gated onto the Data Bus when TRANSMIT DATA is received from the Readout Interface Card Bus Controller (Diag. 10B). The ASCII code uses Data Bus bits as shown in Fig. 1-9. This figure shows the Readout Data Word shifted 5 bits to the left on the Data Bus.

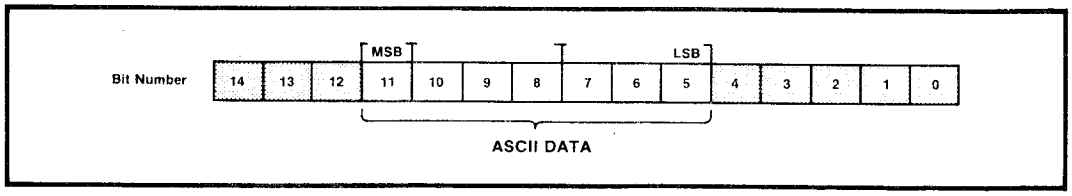

Fig. 1-9. Readout data word.

Display Mode. When the P7001 is in the HOLD mode and waveform information from Memory is being displayed, the ASCII code is read out of Memory and put on the Data Bus. This ASCII code comes into Diag. 10A at top center. It comes down to U52 and U63, the ROM Input Selector. With the STORE input at pins 1 of each selector not asserted (non-store mode), the ASCII code from the Data Bus goes through the ROM Input Latch and to the ROM. In the non-store mode, the ROM takes the ASCII code and converts it to binary numbers representing the number of 0.1 milliamp step units for row and column digital data. In the previous example, ASCII 111010 was for a lower case u. This is converted by the ROM to a binary 0011 (three 0.1 milliamp units of current representing Row 4) and a binary 0010 (two 0.1 milliamp units of current representing Col 2) and sent to

the D-A Converters. The D-A Converters change the binary numbers for row and column current steps to the row and column currents.

The current switches (Q10, Q11, Q20, Q21) are represented in Fig. 1-2 as switch 1. Row 4, column 2 selects the μ symbol in the Readout Board which then sends it to the DPO CRT for display.

Column Force Logic. The column force multiplexer (U62) is used to condense the information sent to the ROM. Any time there is a skip, space, or jump generated by the Readout Board, row Ø information is forced and alternate column-1 information is sent through the ROM Input Selector to the ROM. The column-1 "forced" value is the sum of information on the following four lines which are derived from time slots 1, 2, 3, and 4; row 14; row 10; row 2; row 3; or row 7:

U62 pin 10 has the value 1 derived by: R10+R14+TS1+TS2+TS3
Pin 6 has the value 2 derived by: (R2+R7)·TS1
Pin 3 has the value 4 derived by: (R3)·TS1
Pin 13 has the value 8 derived by: R14

If a character or decimal point command is to be encoded, the Column Force Multiplexer (U62) selects the output of U71, the Column Decimal to Binary Converter. To encode skip, space, or jump, U62 selects the outputs from the Column Force Logic circuits.

By using the Column Force Logic circuits, the other row and column combinations produce the results shown in Fig. 1-10. Table 1-2 is Table 1-1 included again for reference.

Table 1-2

Characters Stored for Timeslot
Dependent Operational Addresses

INPUT CODE		ASCII CHAR STORED IN TIMESLOT 1	2	3	4	5	6	7	8	9	10
SKIPS:	R1, 4-6, 8, 9/CØ	SPACE									
	R2, 7/CØ	;	SPACE		← DELETE →						
	R3/CØ	:	SPACE								
ZEROS LOGIC: R3/C1 thru 4		:									
IDENTIFY: R3/C10		;]	← ILLEGAL INPUT →								
JUMP COMMAND: R14/CØ-10		?									

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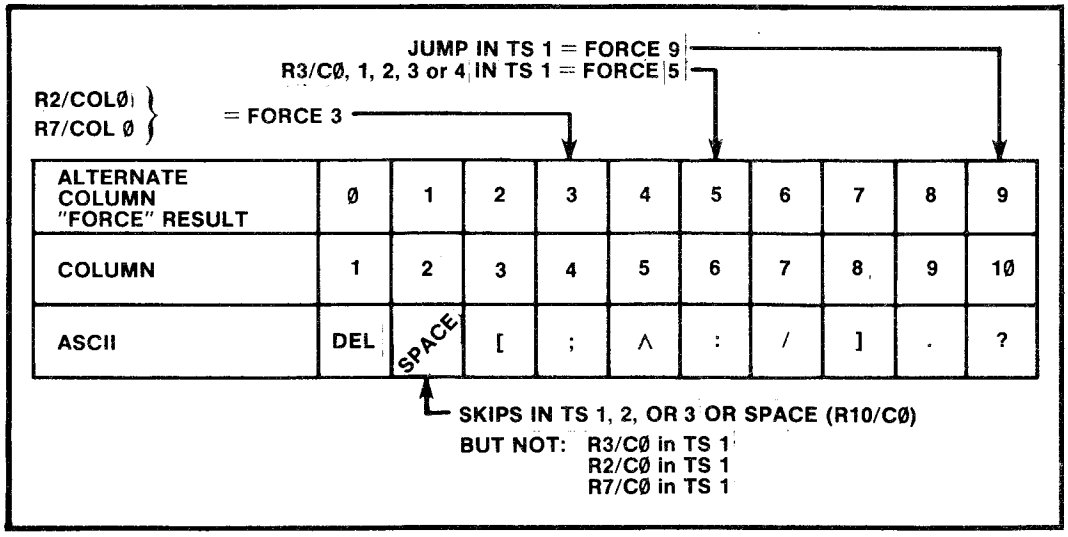

1609-14

Fig. 1-10. "Row Ø" Column Information.

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Examples of Column Force Logic:

1) Skip, (Column Ø, row 1 thru 9) encoded in Timeslot 2:
The Readout Interface encodes a space in TS2 by forcing Row Ø and column 2, storing an ASCII "space" in Memory. DISPLAY SKIP from the Readout Board sets U62 to Ø causing the Readout Interface Card to assume Col Ø instead of using the column data present.

2) Jump (row 14 and any column). Encoded in timeslot 1 (display jumps from one word to the next without displaying the first word): is encoded as an ASCII "?" in TS1.

NOTE

When the JUMP COMMAND exists prior to, during, and after a STORE operation, the contents of timeslots 2 thru 10 will not be addressed. Therefore, the Readout Interface will not write in this area of Memory. Only the first timeslot for the channel with the JUMP COMMAND code, "?", will contain current information.

3) Decimal point character (Row 8, Col 9) encoded in any timeslot:
Since the Row Decimal-to-Binary Converter does not encode Row 8 (or Row 9) information, Row Ø results without forcing Row Ø. Column 9 in Row Ø produces an ASCII ".". Note that this is the only input other than SKIP, SPACE, or JUMP that is treated via Row Ø (Fig. 1-10).

4) Zeros Logic (Row 3, Col 1, 2, 3, or 4) encoded in TS1, 5, 6, or 8:

When the Readout Board receives Row 3, Col 1, 2, 3, or 4 in TS1 from the Plug-ins, it does three things: (1) generates R3, CØ in TS1, (2) generates DISPLAY SKIP in TS1, and (3) remembers the fact that zeros must be added in TS5 or 6 and that the multiplier (µ, m, etc.) may have to be modified in TS8. Three above is dependent upon which column value was sent by the Plug-in (Col 1, 2, 3, or 4).

When the Readout Interface Card receives R3, CØ in TS1, it stores an ASCII colon in the first position in memory by "forcing" Col-1 result or 5. Then the proper zero and multiplier is encoded as received from the Readout Board during TS5, 6, and/or 8.

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Addressing

For each character or operational command, the Readout Interface Card must use the status information to construct an address word of a Memory location for the ASCII code. The following paragraphs describe this procedure.

DPO CRT Readout Location. Up to 80 characters can be displayed on the DPO CRT (see Fig. 1-11, 1-12).

This should not be confused as applying directly to the 80 timeslots per readout frame. Each one of eight groups of ten timeslots cause a display in each one of eight ten-character word positions. Most P7001 Address discussion relates to timeslot information; as opposed to CRT character position within a channel.

For example, the CRT display for one word is: 20 μV. This display could be produced from the Plug-in information as follows:

TIMESLOTS	1	2	3	4	5	6	7	8	9	10
INFORMATION	R3/C1	SKIP	SKIP	2	SKIP	SKIP	SKIP	μ	V	SKIP

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The same display (20 μV) could be produced from the ASCII information stored in P7001 memory as follows:

MEMORY LOCATION	1	2	3	4	5	6	7	8	9	10
ASCII INFORMATION	:	SPACE	SPACE	2	DEL	DEL	DEL	u	V	DEL

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During STORE, the Readout Interface card receives the results of a zero's logic command rather than data as encoded by the Plug-ins.

Word Character Positions. The P7001 Readout Interface Word Channels are numbered in the order shown in Fig. 1-11 to allow an external controller (computer or calculator) to write messages in sequence in Memory. When readout from Memory occurs by the Readout Interface, it uses the Channel address information (Fig. 1-14) from the Acquisition Unit to locate the ASCII code in Memory. This procedure is discussed further under the paragraph titled "Address Word Composition".

NOTE

When generating messages there is a one-to-one correspondence between character positions and timeslots only if the ASCII codes used are those shown in Fig. 1-7. Of the codes shown in Fig. 1-8 are used, their location in the word position is critical and will cause operational addresses to be sent to the Readout Board.

The P7001 stores information for all 80 timeslots for each selected waveform (A, B, C, D) of the given Field. When a 4k Memory is installed, an external controller can access three other Readout Fields and store another 80 characters for each waveform in each field. Fig. 1-12 is a Memory Address Map of the 4k Memory. Each of the blocks (Field Ø, block A, for example) shown on the bottom half of the figure contains up to 80 readout characters. Each Memory address contains information for one timeslot (one seven-bit ASCII word).

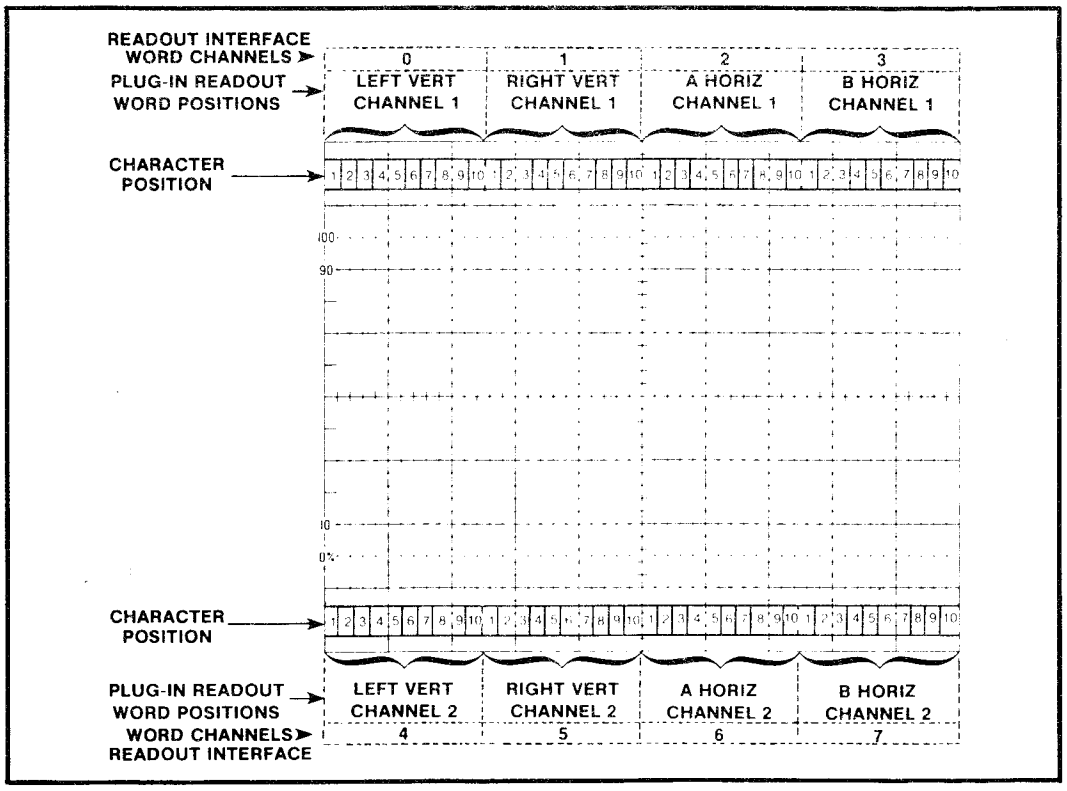

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Fig. 1-11. DPO CRT readout location.

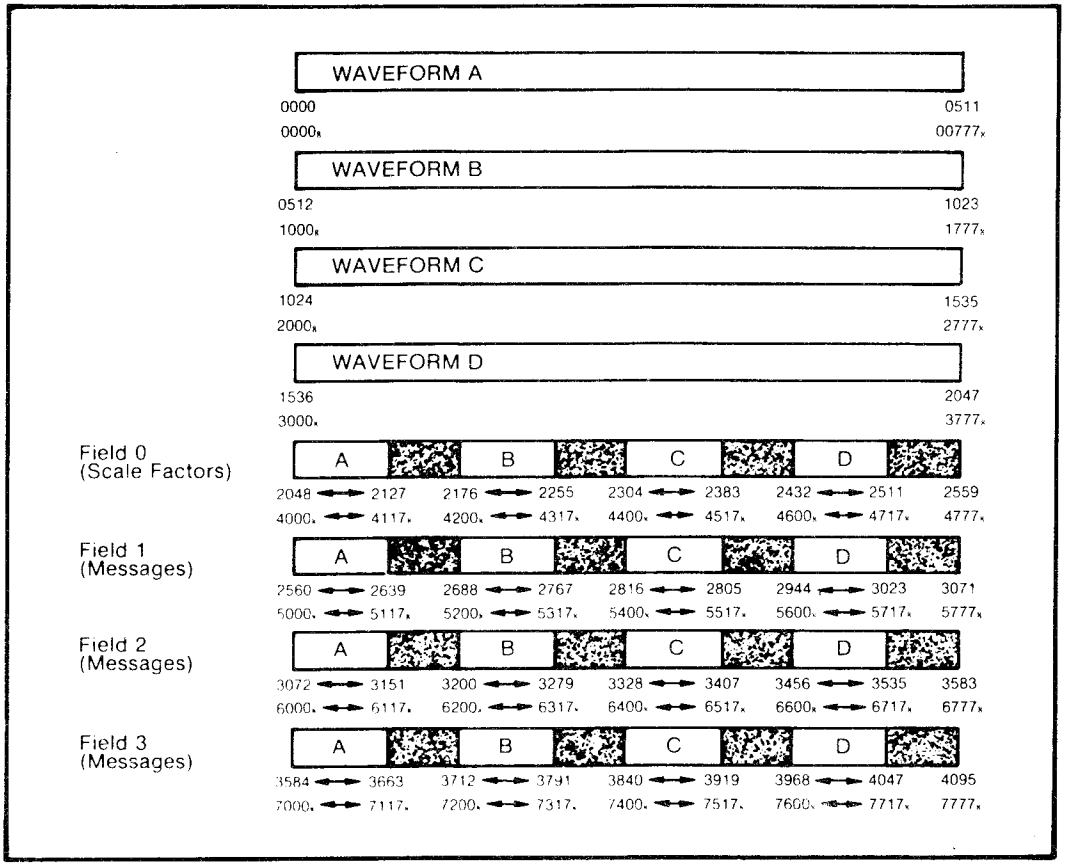

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Fig. 1-12. P7001 Memory address map.

Address Word Composition. Addressing is a matter of composing an address word used to determine where in Memory each seven bit ASCII code will be stored. Three groups of information are used to build the address word; Channel and Timeslot bits, Waveform bits, and Field address bits. The format of this word is shown in Fig. 1-13.

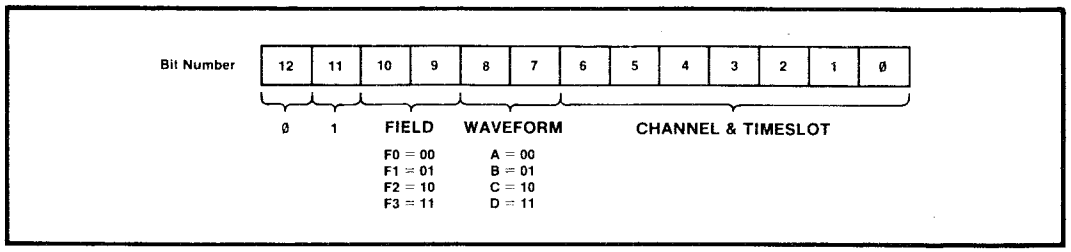

Fig. 1-13. Readout memory address word format.

Channel and Timeslot Bits. Channel and timeslot bits, bits Ø thru 6 of the Readout Memory Address Word (Fig. 1-13), are derived from two groups of information: Channel Address (CH ADD) and timeslots (TS). The Readout Interface timeslot counter (U25, Diag. 10B) is a Decade counter which is advanced for each falling edge of TRIGGER, and reset (to TS1) each time that the channel address advances. The output of U25 is in Binary Coded Decimal (BCD), where Ø thru 9 represent timeslots 1 thru 10. This gives us the term "timeslot-1 or TS-1".

Channel address line, $\overline{\text{CH ADD 1}}$ from the Acquisition Unit has been inverted at the input to the Readout Interface card, to provide CH ADD 1. CH ADD 1, CH ADD 2 and CH ADD 4 have been rearranged and assigned a BCD weighting (Fig. 1-14 and 1-15). This BCD value becomes the Most Significant Digit (MSD) of the channel and timeslot portion of the Readout Memory Address Word, and the timeslot-1 BCD value becomes the Least Significant Digit (LSD). The BCD result

(MSD + LDS) is then converted to binary to produce contiguous readout address groups in Memory. The Readout Interface takes readout data from Memory in a zig-zag sequence, however, since the channel counts used by the Readout Board to address the Plug-ins is also used to make up the Memory address by the Readout Interface Card.

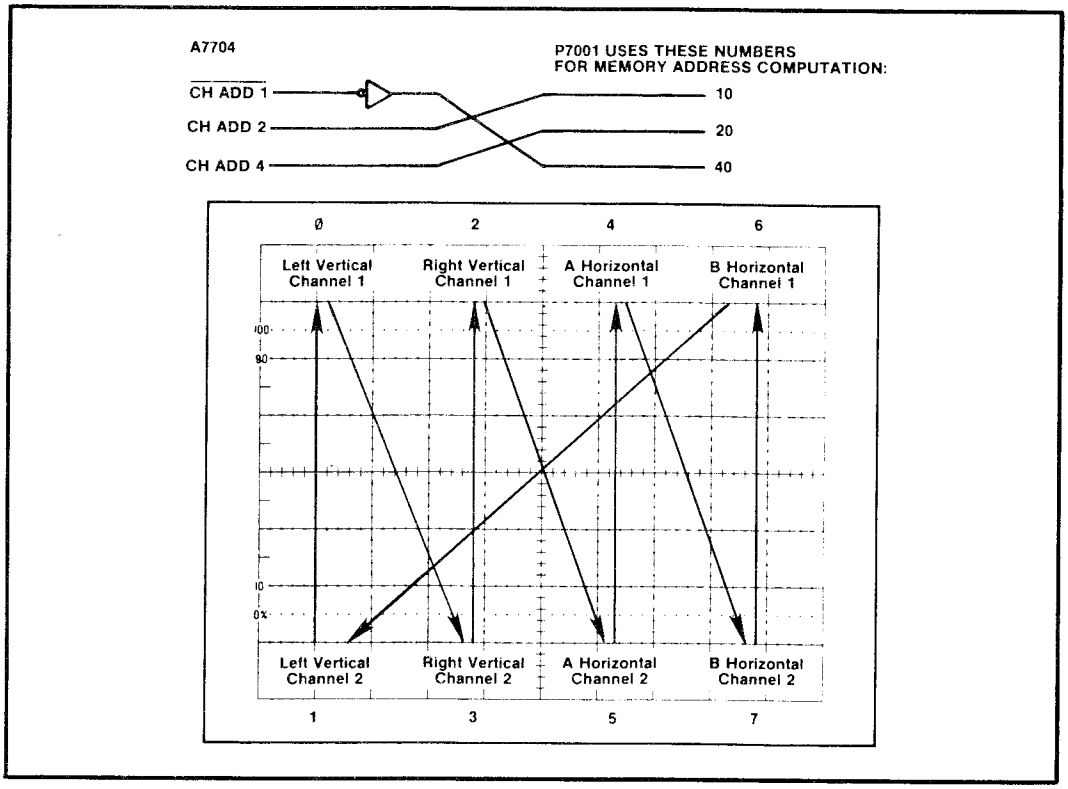

Fig. 1-14. Channel address sequence.

PLUG-IN READOUT WORD POSITION	7704A CH ADD 4	7704A CH ADD 2	7704A $\overline{\text{CH ADD 1}}$	7704A CHANNEL ADDRESS	P7001 MEMORY CH START ADDRESS BCD	P7001 MEMORY CH START ADDRESS OCTAL
LEFT VERT CH 2	LO	LO	LO	1	40	50_8
LEFT VERT CH 1	LO	LO	HI	0	00	00_8
RIGHT VERT CH 2	LO	HI	LO	3	50	62_8
RIGHT VERT CH 1	LO	HI	HI	2	10	12_8
A HORIZ CH 2	HI	LO	LO	5	60	74_8
A HORIZ CH 1	HI	LO	HI	4	20	24_8
B HORIZ CH 2	HI	HI	LO	7	70	106_8
B HORIZ CH 1	HI	HI	HI	6	30	36_8

1609-20

Fig. 1-15. Channel address code - From A7704. (See also Table 2-3, page 2-48, of the 7704A Service Manual.)

Status Word. The Field and Waveform information for address word composition is determined by the Readout Interface Card Status Word. The Status Word is latched into the Readout Interface Card Status Latches (U74 and U54A). The Status Word is sent on the Data Bus by either the Front Panel or an external controller. The Status Latches remain set until changed by a new status word.

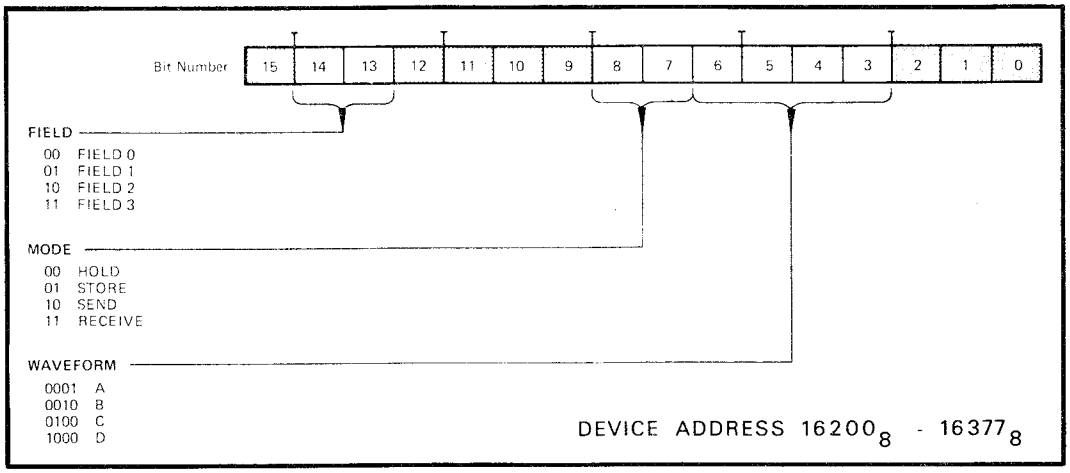

Fig. 1-16. Readout Interface status word format.

U74 (Diag. 10B) holds bits 13 and 14 (Field Information) and bits 3, 4, 5, and 6 (Waveform Information). U74 is cleared through pin 1 by $\overline{\text{POWER FAIL}}$ when the instrument is first turned on, setting its status to Field Ø, HOLD, and Waveform A, B, C, D (Fig. 1-16). The waveform counter selects readout for waveform A for display. $\overline{\text{STATUS STROBE}}$ clocks the Status Word from the Data Bus through U55D and U45C (when $\overline{\text{DATA MODE Ø}}$ is LO) to pin 9 of U74. $\overline{\text{STATUS STROBE}}$ is sent shortly after the Status Word is settled on the Data Bus. The Status Word can also be latched into the status latches when the card is addressed by an external controller.

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Field Address Bits. Bits 13 and 14 of the Status Word become Readout Memory Address Word bits 9 and 10, and are gated on the Address Bus when LOAD BUS is sent by the Readout Interface Bus Controller.

Bits 13 and 14 are set to a state other than Ø only by an external controller. If a Status Word is sent from the front panel, the bits remain Ø, Ø which indicates Field Ø. So any time we use the front panel buttons to change status, we display and store readout information from/to Field Ø only.

Mode. There are two basic modes of the Readout Interface Card: HOLD and STORE. No action is taken by the Readout Interface Card during SEND or RECEIVE. The Mode is recognized by STORE Status Latch U54A which in its set (Ø) state indicates HOLD. $\overline{\text{BIT 7}\cdot\text{BIT 8}}$ combination is the D input to U54A and when true (active low) will set U54A to STORE.

The STORE signal goes to inverter U43B where it will limit the voltage level on the READOUT INTENSITY line at Q45 and also on the A7704 Readout Board. This means that when we're in the STORE mode, the Readout Intensity cannot be turned off and Readout Data will be stored in Memory.

Waveform Address Bits. Bits 3, 4, 5, and 6 of the Status Word are decoded to become bits 7 and 8 of the Readout Memory Address Word. The Readout Interface Card must be able to address up to four different waveform address areas during STORE, or just one waveform (selected waveform nearest to A) during HOLD. A special

waveform counter (U94A and U94B) is used to generate one of four binary combinations for the two waveform address bits (bits 7 and 8 of the memory address word). The counter starts with a count of Ø (waveform A) and can advance at the end of each readout frame (indicated by a negative transition of CH ADD 4). During HOLD mode, the counter will stop at the first selected "VALID" waveform determined by status latch U74. During STORE mode, the counter will advance after each readout frame. However, a STORE operation will occur only for VALID waveforms.

A waveform comparator (U84) is used to determine if a given waveform (as indicated by the waveform counter) is valid. The comparator outputs a VALID signal if the selected input is connected to an active "low" waveform status output line.

Summary. In the past several paragraphs, we have shown the sources of information which make up the Readout memory address word (Fig. 1-17). This word is used by the Readout Interface Card to determine the location of the ASCII data in the P7001 Memory, whether storing or retrieving data. Figure 1-18 gives examples of the Readout Memory Address Word. Compare this figure with Fig. 1-19 which shows the four waveform addresses along with their readout data addresses.

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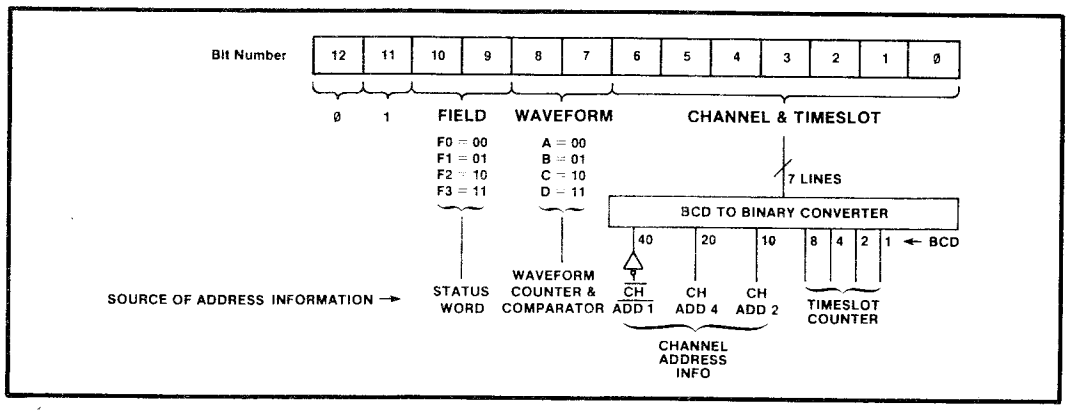


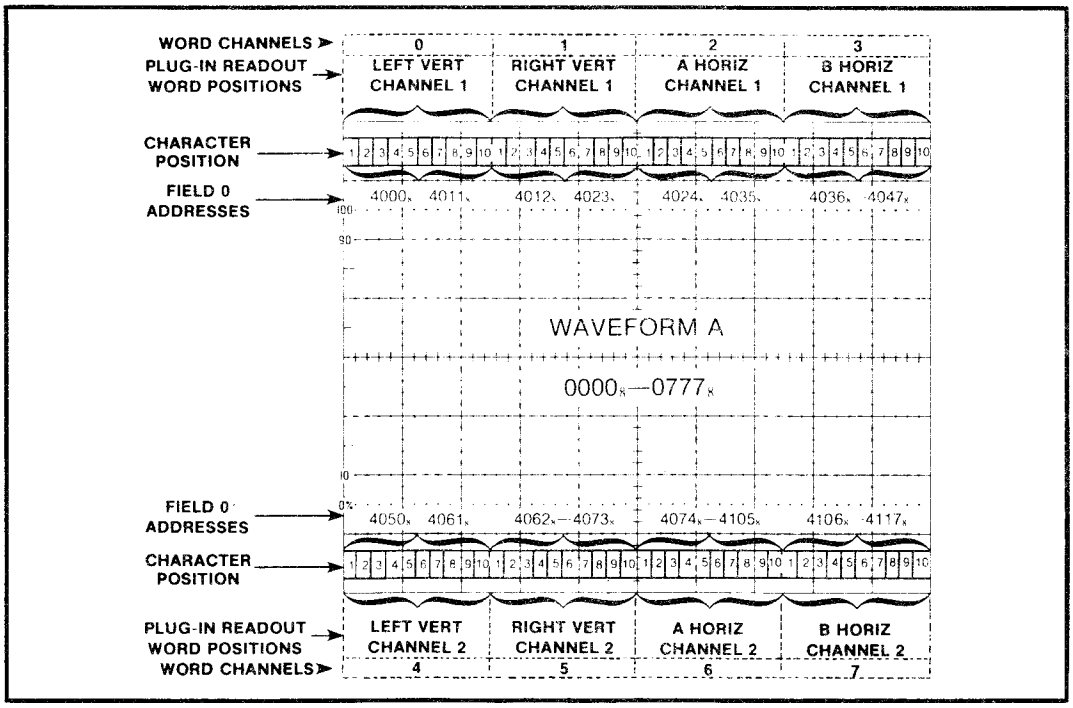
1609-22

Fig. 1-17. Readout memory address word with source of address information.

PIN NUMBER	A25	B24	A24	B23	A23	B22	A22	B21	A21	B20	A20	B19	A19	
BIT NUMBER	12	11	10	9	8	7	6	5	4	3	2	1	0	
FUNCTION	SET TO Ø	SET TO 1	FIELD		WAVE FORM		CHANNEL & TIMESLOTS							
BINARY	Ø	1	Ø	1	1	1	Ø	1	Ø	Ø	1	Ø	1	WAVEFORM D, FIELD 3, WORD CHAN 3, AND TIMESLOT 8.
OCTAL			5			6			4			5_8		
BINARY	Ø	1	1	1	1	1	1	Ø	Ø	1	Ø	1	Ø	WAVEFORM D, FIELD 3, WORD CHAN 7, AND TIMESLOT 5.
OCTAL			7			7			1			2_8		

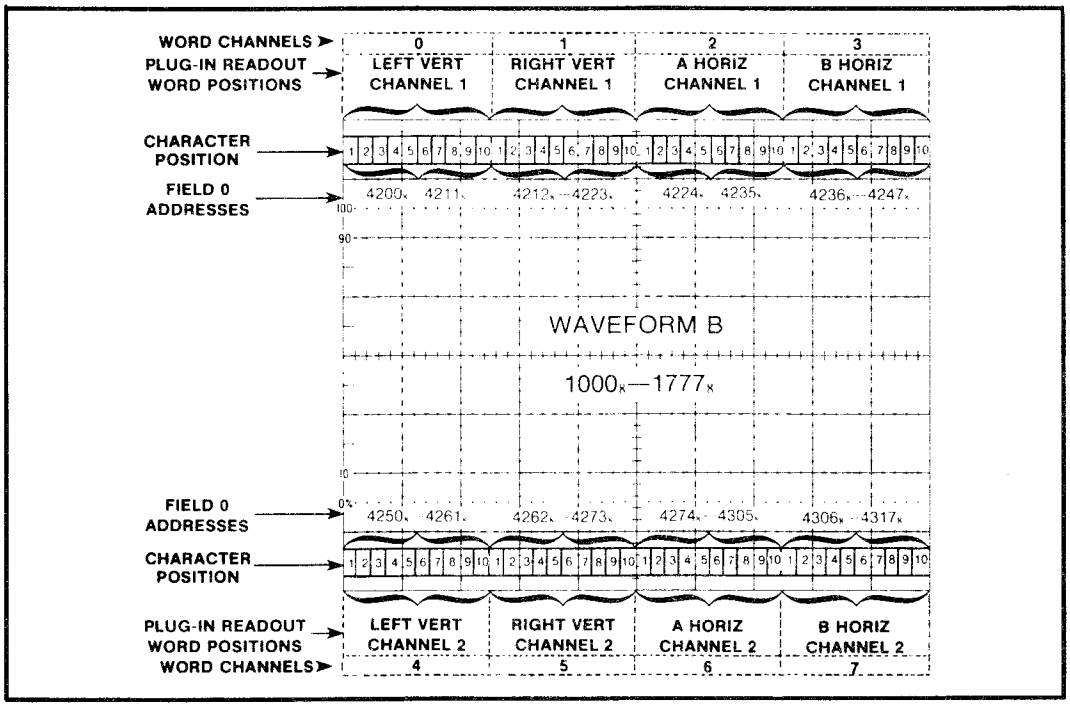
1609-23

Fig. 1-18. Readout Address Word examples.



1609-24

Fig. 1-19a. Readout Addresses for Waveform A, Field Ø.



1609-25

Fig. 1-19b. Readout Addresses for Waveform B, Field Ø.

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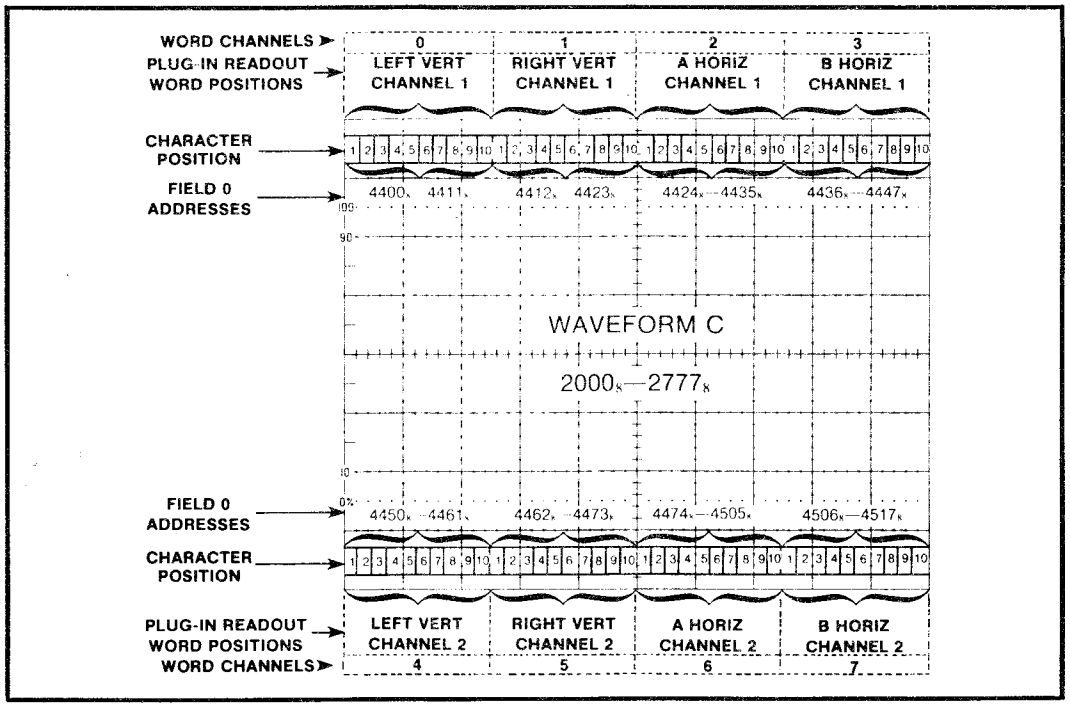
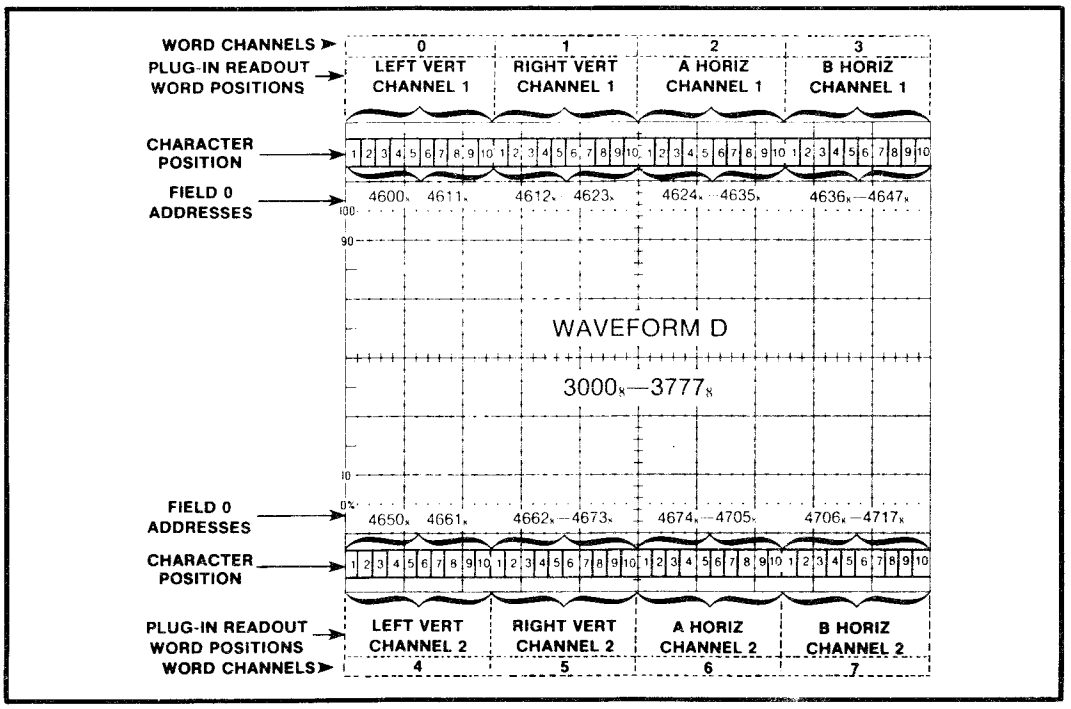


1609-26

Fig. 1-19c. Readout Addresses for Waveform C, Field Ø.



1609-27

Fig. 1-19d. Readout Addresses for Waveform D, Field Ø.

Timing

A certain amount of time is required to either store or read ASCII data to/from the Memory. The process of A-D and D-A conversion, decimal to binary conversion, zeros logic determination, ROM Input Selection, conversion by the ROM to/from ASCII, and loading the Bus all require time. Timing is accomplished by the timing circuits on Diag. 10A.

The READOUT TRIGGER coming in at pin A33, Diag. 10A, has an amplitude of about 5V and a period of about 250 microseconds. This period changes to about 210 microseconds when no character is being written. Rise/Fall time of this trigger is slow and it may have noise spikes on it, causing the TTL circuits to respond at the wrong time. Emitter follower, Q01, passes the trigger on to the D input of flip-flop U64A. The two flip-flops (U64A and B) are used to "clean up" this trigger pulse. The Clock, U85B, has a 1.2 microsecond period output at pin 5. This 1.2 microsecond pulse clocks the rising edge of the trigger pulse into flip-flop U64A. The next 1.2 microsecond pulse clocks it on into U64B. Since the input signal should have completed a transition in less than 1.2 microseconds -- although the signal may make many transitions or oscillate during that time -- a single, fast positive output transition will result. The output may be delayed 1.2 to 2.4 microseconds. A HIGH state continues as long as READOUT TRIGGER is high. When the trigger starts to go low, the 1.2 microsecond pulse turns off U64A and B and produces a single negative output transition. This gives a trigger pulse with fast rise and fall times and ignores any transition noise on the input trigger pulse.

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TRIGGER (pin 7, U64B) drives the Timeslot Counter (Diag. 10B). The rising edge of this signal also fires the Display Time One Shot U85A. The $\overline{Q}$ output from U85A stays low for approximately 20 microseconds to allow for full character output. At the end of this time, the rising edge of DISPLAY TIME clocks U93B, setting INHIBIT R&C OUTPUT HI. U93B will stay HI until the next STROBE is received, clearing U93B. Fig. 1-20 shows the timing of the Readout Interface Circuits during the display mode.

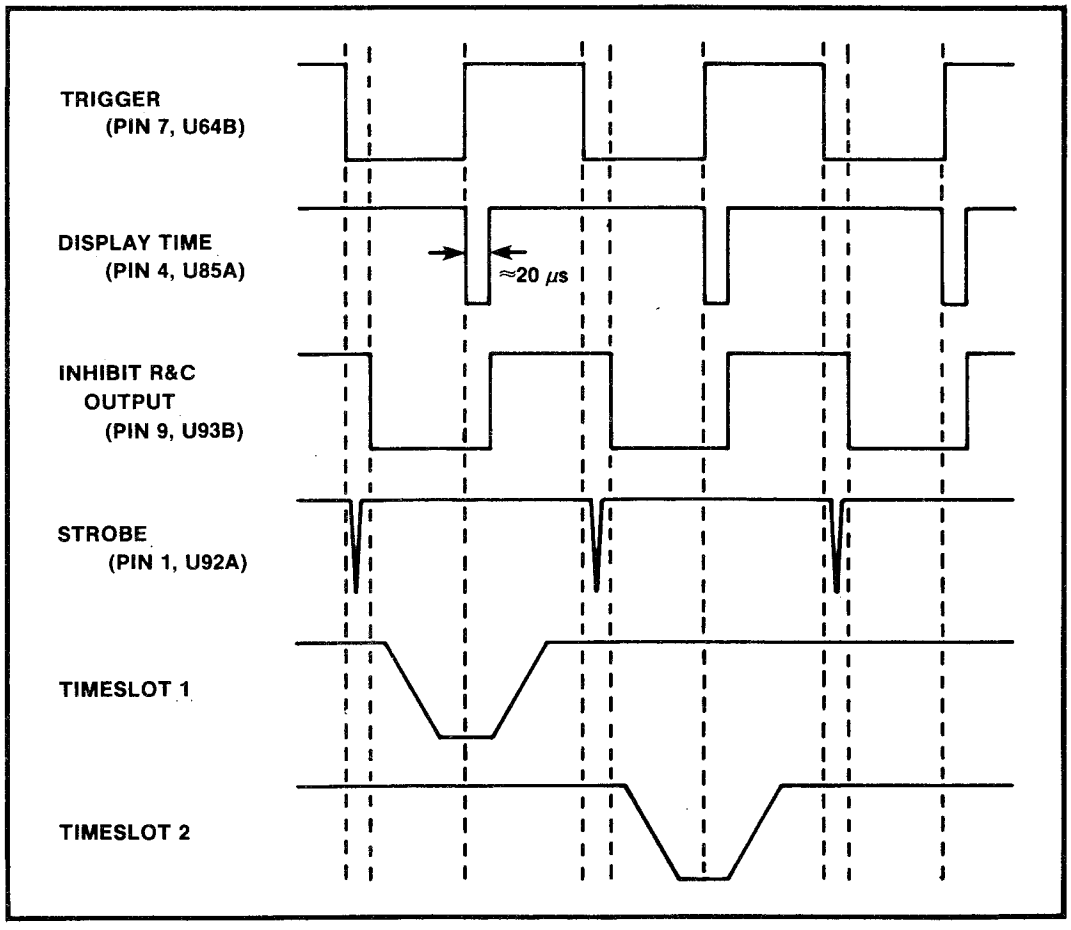

Fig. 1-20. Readout Interface timing (DISPLAY mode).

Bus Control. Along the bottom of Diag. 10B is the Bus Controller circuitry. The truth table, shown to the right of U95C, indicates the status of the controller flip-flops during their four states.

Starting from the idle state, the first position of the truth table, the request cycle is started by an interrupt generated by Interrupt Generator U93A. This is done only if both inputs to U82B are high. U82B inputs are both high during STORE and when VALID is HI. They are also both high when VALID is HI and the Readout Intensity control on the Display Unit (D7704) is on. The interrupt signal from U93A clears U91A. This sets the controller to the Bus Request state, the second position on the truth table. The two highs (U91B, pin 8 and U91A, pin 6) satisfy the inputs to AND gate U15D. This sends a LO out to the Front Panel Priority logic circuit on the Front Panel Card. The Front Panel Priority Logic will send out DATA CH GRANT. If a card with a higher priority request the bus, it will stop DATA CH GRANT. If not, then when DATA CH GRANT arrives at the Readout Interface Card, pin B13, it clocks U91B switching it to the 1 state. We're now in the SEL ACK state of the Bus Controller. U05D passes the state (SEL ACK) to card pin B15. This turns off DATA CH GRANT. U44A looks at $\overline{\text{SYNC ACK}}$, $\overline{\text{BUS BUSY}}$, and $\overline{Q}$ of U91A and generates a LO to U75A. At the time DATA CH GRANT is lifted, U91A clocks to its 1 state. The Bus Controller is then in the Master state, line four on the truth table.

In the Master State, U95D generates LOAD BUS, BUS BUSY, and TRANSMIT DATA (during a valid STORE). LOAD BUS is used to gate the

address on the Address Bus during STORE and HOLD. TRANSMIT DATA is used to gate the ASCII data on the Data Bus during STORE only.

$\overline{\text{SYNC ACK}}$ is generated by the Memory after a Readout Display cycle, or by U05B (Readout Interface Card) after being addressed by an external controller or on receipt of STATUS STROBE from the Front Panel. $\overline{\text{SYNC ACK}}$ resets the Bus Controller (U91A and U91B) to its idle state through U75B, U82C, U92A, and U92B.

In the HOLD mode (DISPLAY), STROBE INTERRUPT, generated by the timing circuits, arrives after the negative transition of Readout Trigger. For the STORE mode it arrives after the positive transition of the Readout Trigger.

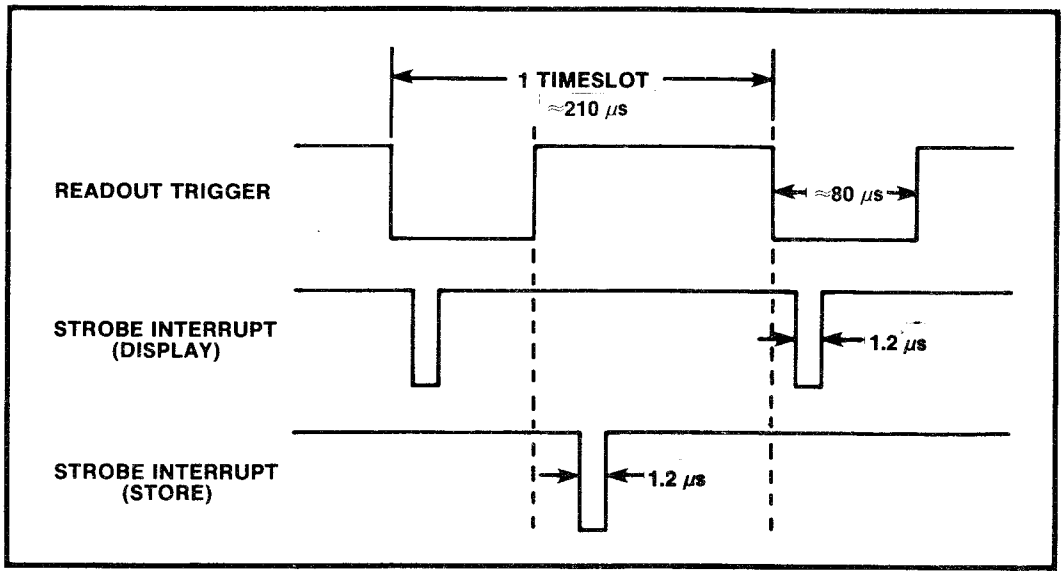

Fig. 1-21. Strobe interrupt timing.

Using STROBE INTERRUPT, the Readout Interface Card Bus Controller request the Bus as often as needed to display all characters from Memory or store all characters from the Acquisition Unit.

During Display from Memory, the process is continued to keep the CRT display refreshed. During STORE the process continues storing in Memory until set to the HOLD mode.

Readout Intensity. Bus transfers from Memory to the Readout Interface Card will not occur in the HOLD mode, if the Readout Intensity control on the Display Unit is off. When this control is turned off, a positive voltage is placed on card pin B1 (Diag. 10B). This positive voltage turns on Q45, pulling U82B input, pin 4, low. The D input to U93A will therefore remain low. Then when STROBE INTERRUPT clocks U93A, the Bus Controller, U91A, will not reset. This holds the Bus Controller in the idle state. During a STORE operation, the Readout Interface will override an OFF condition of the control on the Display Unit by preventing the Readout Intensity line from going positive. The Readout Board must be "on" during a STORE mode of the Readout Interface Card. This is to allow the Operational commands to be processed prior to action by the Readout Interface Card.

SECTION 2

MAINTENANCE

Calibration

Calibration of the Readout Interface Card involves two adjustments, R90 (ROW) and R91 (COLUMN), both of which are shown on Diag. 10A.

Equipment Required.

1 - Tektronix 7A16A Amplifier (or other Amplifier with readout)

1 - Tektronix 7B70 or 7B71 Time-Base Unit (or other Time-Base Unit with readout)

1 - Adjusting Tool (small screwdriver)

Procedures:

1. Switch DPO Power off.

2. Open the front panel by removing the four Phillip screws. Slowly pull the panel out about one inch and then swing it to the left.

3. The Readout Interface Card is located in the center of the P7001. R90 (Row), and R91 (COLUMN), are marked near the front edge of the card.

4. Set the P7001 Front Panel as follows:

   Data Handling STORE

Memory Location	A, START
Display Source	MEMORY

5. Install a Time-Base Unit (7B71) in one of the horizontal compartments and set its controls as follows:

   Non-Amplifier

Time/Div	0.1 milliseconds/Div

6. Install an Amplifier (7A16A) in one of the vertical compartments and set its controls as follows:

Polarity	Invert
Volts/Div	.5V

   Set Volts/Div to variable -- (out)

   Ground Input Coupling Switch

7. Set the Mainframe Vert and Horiz Mode switches to correspond to the proper location.

8. Turn on the DPO and wait at least 20 minutes.

9. Adjust R90 in one direction while alternately pressing STORE and START until incorrect readout occurs (wrong or distorted characters). Note the position of the control. Rotate the control in the opposite direction beyond the region of proper operation until incorrect readout occurs. Note the position. Set the control in the physical center of its rotation between these two positions. Adjust R91 in the same manner.

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NOTE

If a change to an incorrect readout display cannot be achieved, set the control to the physical center of its range.

10. Secure the Front Panel with the four Phillips screws.

Troubleshooting Hints

Troubleshooting requires a good understanding of the operation of the Readout Interface Card. The following key points have been noted to aid in trouble isolation.

1. Check the status of the Bus Controller with the Truth Table on diagram 10B. Check U91 A and B, pin nine and five.

2. Check the timing during HOLD (Display) shown in Figures 1-20 and 1-21.

3. The outputs from the ROM swing from about -0.7V to +5V.

REPLACEABLE PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX MFR. CODE NUMBER TO MANUFACTURER

MFR.CODE	MANUFACTURER	ADDRESS	CITY,STATE,ZIP
01121	ALLEN-BRADLEY CO.	1201 2ND ST. SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P. O. BOX 5012	DALLAS, TX 75222
03508	GENERAL ELECTRIC CO., SEMI-CONDUCTOR PRODUCTS DEPT.	ELECTRONICS PARK	SYRACUSE, NY 13201
04713	MOTOROLA, INC., SEMICONDUCTOR PRODUCTS DIV.	5005 E. MCDOWELL RD.	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS ST.	MOUNTAIN VIEW, CA 94042
07910	TELEDYNE SEMICONDUCTOR	12515 CHADRON AVE.	HAWTHORNE, CA 90250
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON ST.	DOVER, NH 03820
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
18677	SCANBE MFG. CORP.	3445 FLETCHER AVE.	EL MONTE, CA 91731
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SAN YSIDRO WAY	SANTA CLARA, CA 95051
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BlVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P. O. BOX 500	BEAVERTON, OR 97077
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY CO., INC.	3029 E. WASHINGTON ST.	INDIANAPOLIS, IN 46206

ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
	670-2385-00			CKT BOARD ASSY: READOUT	80009	670-2385-00
C01	290-0527-00			CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020NLF
C03	290-0530-00			CAP.,FXD,ELCTLT:68UF,20%,6V	90201	TDC686M006NLF
C05	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C07	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C09	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C10	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C12	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C13	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C15	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C16	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C17	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C18	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C19	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C20	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C21	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-547E103Z
C25	290-0527-00			CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020NLF
C28	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
C34	283-0110-00			CAP.,FXD,CER DI:0.005UF,+80-20%,150V	56289	19C242B
C45	283-0150-00			CAP.,FXD,CER DI:650PF,5%,200V	72982	835-515B651J
C47	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
C70	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
C81	281-0543-00			CAP.,FXD,CER DI:270PF,10%,500V	72982	301-055X5P1271K
C83	283-0110-00			CAP.,FXD,CER DI:0.005UF,+80-20%,150V	56289	19C242B
C85	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
CR24	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR41	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR42	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR65	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR90	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR95	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
Q10	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00
Q11	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00
Q20	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00
Q21	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00
Q45	151-0281-00			TRANSISTOR:SILICON,NPN	03508	X16P4039
Q51	151-0188-00			TRANSISTOR:SILICON,PNP	04713	2N3906
R05	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R10	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R12	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R13	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R14	307-0383-00			RES.,FXD,FILM:4.7 OHM,2%,1.5W	73138	899-1-R4.7K
R21	321-0312-00			RES.,FXD,FILM:17.4K OHM,1%,0125W	75042	CEAT0-1742F
R23	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	75042	CEAT0-3482F
R24	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R25	321-0370-00			RES.,FXD,FILM:69.8K OHM,1%,0.125W	75042	CEAT0-6982F
R27	321-0381-00			RES.,FXD,FILM:90.9K OHM,1%,0.125W	75042	CEAT0-9092F
R28	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R29	321-0262-00			RES.,FXD,FILM:5.23K OHM,1%,0.125W	75042	CEAT0-5231F
R30	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R31	321-0312-00			RES.,FXD,FILM:17.4K OHM,1%,0125W	75042	CEAT0-1742F

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R33	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	75042	CEAT0-3482F
R34	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R35	321-0370-00			RES.,FXD,FILM:69.8K OHM,1%,0.125W	75042	CEAT0-6982F
R36	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
R37	321-0381-00			RES.,FXD,FILM:90.9K OHM,1%,0.125W	75042	CEAT0-9092F
R39	321-0262-00			RES.,FXD,FILM:5.23K OHM,1%,0.125W	75042	CEAT0-5231F
R40	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
R42	321-0329-00			RES.,FXD,FILM:26.1K OHM,1%,0.125W	75042	CEAT0-2612F
R43	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R44	321-0303-00			RES.,FXD,FILM:14K OHM,1%,0.125W	75042	CEAT0-1402F
R45	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R46	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R47	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R48	315-0912-00			RES.,FXD,CMPSN:9.1K OHM,5%,0.25W	01121	CB9125
R51	307-0387-00			RES.,FXD,FILM:13 RES.NETWORK,8200 OHM	73138	899-1-R8.2K
R53	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R57	321-0259-00			RES.,FXD,FILM:4.87K OHM,1%,0.125W	12697	MFF1816G48700F
R59	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R60	307-0387-00			RES.,FXD,FILM:13 RES.NETWORK,8200 OHM	73138	899-1-R8.2K
R62	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R63	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R64	315-0912-00			RES.,FXD,CMPSN:9.1K OHM,5%,0.25W	01121	CB9125
R65	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R67	315-0912-00			RES.,FXD,CMPSN:9.1K OHM,5%,0.25W	01121	CB9125
R73	321-0259-00			RES.,FXD,FILM:4.87K OHM,1%,0.125W	12697	MFF1816G48700F
R77	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R79	301-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.50W	01121	EB3925
R81	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R83	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R85	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R90	311-1248-00			RES.,VAR,NONWIR:500 OHM,10%,0.50W	73138	72X-23-0-501K
R91	311-1248-00			RES.,VAR,NONWIR:500 OHM,10%,0.50W	73138	72X-23-0-501K
R93	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R95	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
R96	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R97	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
R98	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R99	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
U01	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U02	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U03	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U04	156-0315-00			MICROCIRCUIT,DI:BCD +O BINARYCONV	01295	SN74184N
U05	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U12	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U13	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U15	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U21	155-0038-01			MICROCIRCUIT,DI:5-BIT DGTL +OANLG CONV	80009	155-0038-01
U22	156-0058-00			MICROCIRCUIT,DI:HEX INVERTER	04713	MC7404P
U23	156-0058-00			MICROCIRCUIT,DI:HEX INVERTER	04713	MC7404P
U24	156-0315-00			MICROCIRCUIT,DI:BCD +O BINARYCONV	01295	SN74184N
U25	156-0079-00			MICROCIRCUIT,DI:DECADE COUNTER,TTL	07263	9390PC
U31	155-0038-01			MICROCIRCUIT,DI:5-BIT DGTL +OANLG CONV	80009	155-0038-01
U32	156-0346-00			MICROCIRCUIT,DI:READ-ONLY-MEMORY	34649	1302-0155

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U33	156-0043-00			MICROCIRCUIT,DI:2-INPUT NOR GATE	01295	SN7402N
U34	156-0058-00			MICROCIRCUIT,DI:HEX INVERTER	04713	MC7404P
U40	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	S5558V
U43	156-0058-00			MICROCIRCUIT,DI:HEX INVERTER	04713	MC7404P
U44	156-0047-00			MICROCIRCUIT,DI:3-INPUT NAND GATE	01295	SN7410N
U45	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN7408N
U50	155-0014-01			MICROCIRCUIT,DI:ML,ANALOG TO DECIMAL CONV	80009	155-0014-01
U52	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN74157N
U53	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	01295	SN74174N
U54	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U55	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U61	156-0219-00			MICROCIRCUIT,DI:8-INPUT PRIORITY DCDR	07263	9318DC
U62	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN74157N
U63	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN74157N
U64	156-0221-00			MICROCIRCUIT,DI:QUAD LATCH	01295	SN74175N
U65	156-0062-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS EXCL GATE	04713	MC7486P
U70	155-0014-01			MICROCIRCUIT,DI:ML,ANALOG TO DECIMAL CONV	80009	155-0014-01
U71	156-0347-00			MICROCIRCUIT,DI:10-LINE TO 4-LINE ENCODER	01295	SN74147N
U72	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U73	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U74	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	01295	SN74174N
U75	156-0043-00			MICROCIRCUIT,DI:2-INPUT NOR GATE	01295	SN7402N
U81	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	01295	SN7408N
U82	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U83	156-0043-00			MICROCIRCUIT,DI:2-INPUT NOR GATE	01295	SN7402N
U84	156-0075-00			MICROCIRCUIT,DI:SNGL 8-BIT DATA SEL MUX	01295	SN74151N
U85	156-0172-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	01295	SN74123N
U91	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U92	156-0043-00			MICROCIRCUIT,DI:2-INPUT NOR GATE	01295	SN7402N
U93	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U94	156-0039-00			MICROCIRCUIT,DI:DUAL J-K FLIP FLOP	01295	SN7473N
U95	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
VR11	152-0309-00			SEMICOND DEVICE:ZENER,1W,6.2V,5%	04713	1N3828A
VR50	152-0127-00			SEMICOND DEVICE:ZENER,0.4W,7.5V,5%	04713	1N755A
VR70	152-0168-00			SEMICOND DEVICE:ZENER,0.4W,12V,5%	04713	1N963B

MECHANICAL PARTS

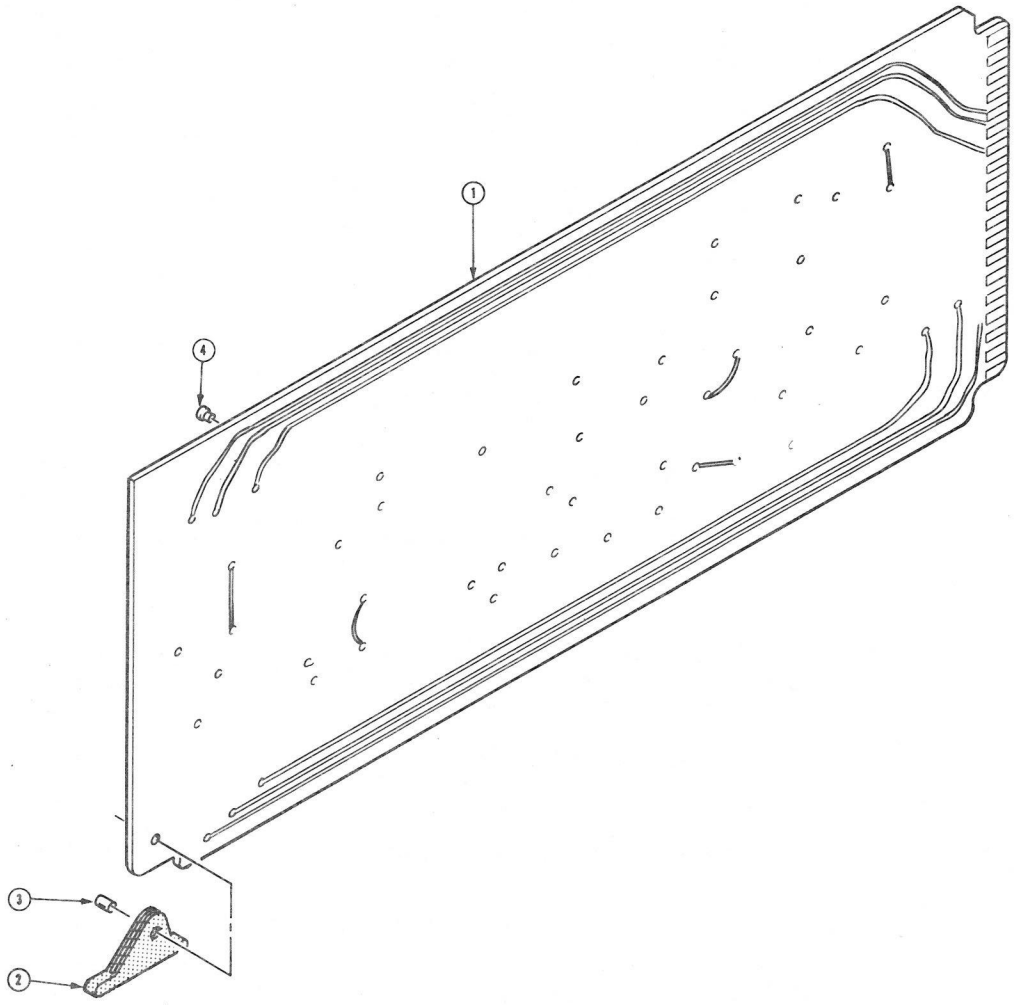
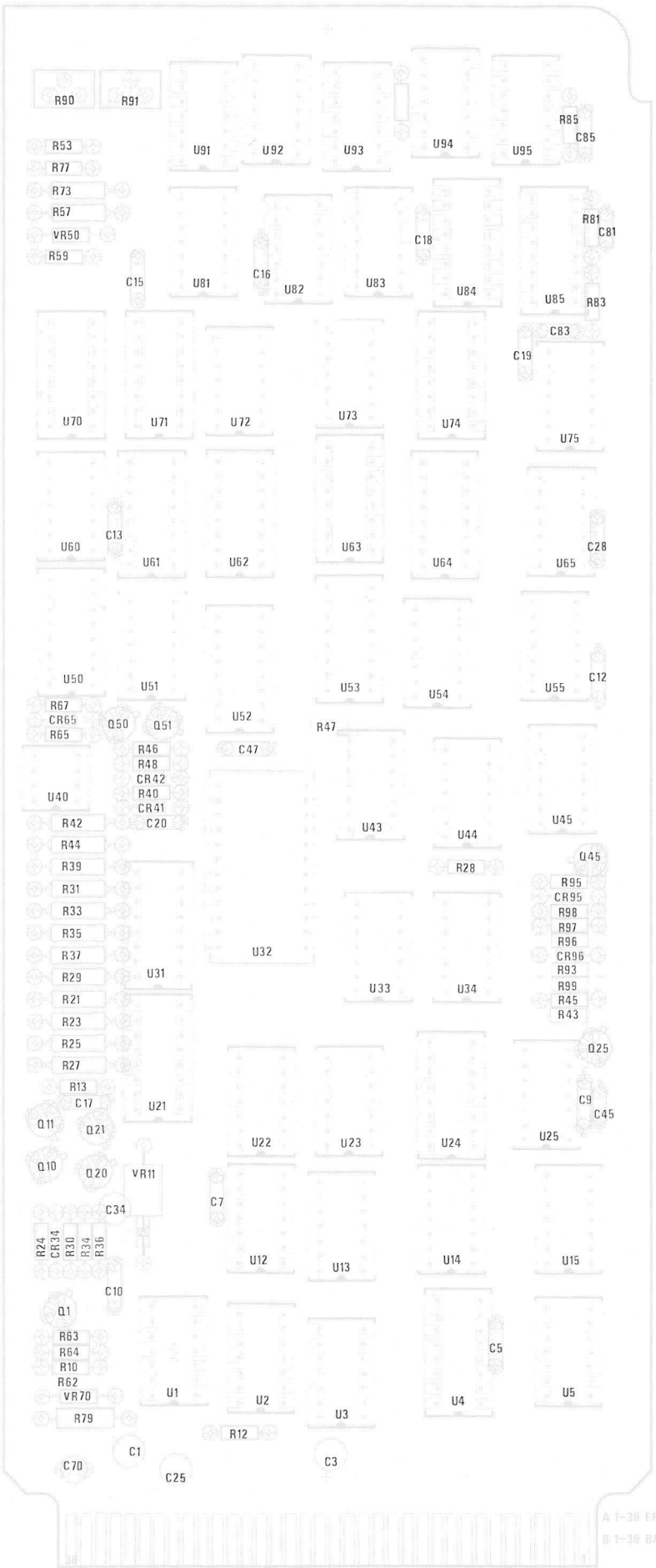
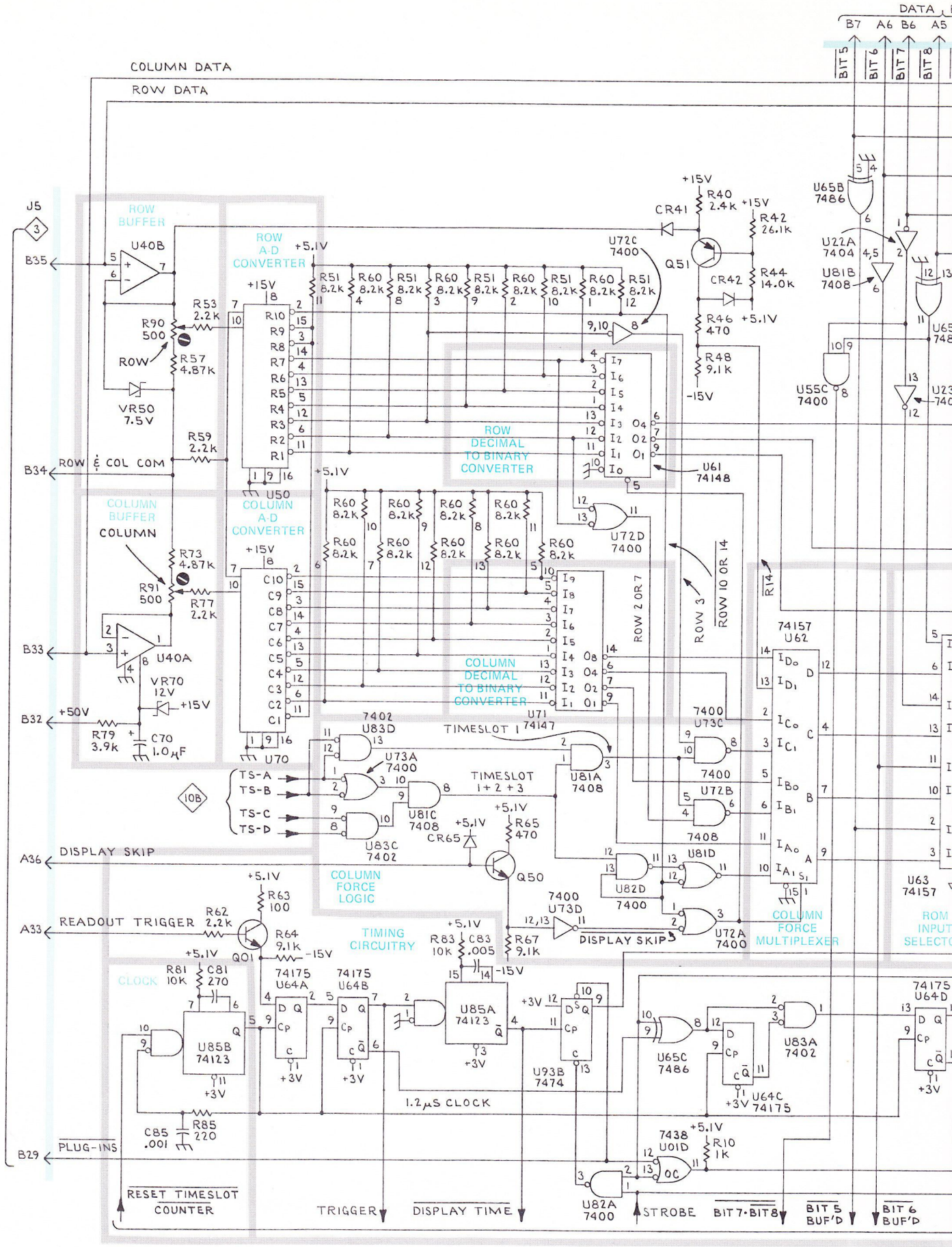


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	----- -----			1		CKT BOARD ASSY:READOUT(SEE EPL)		
-2	105-0144-00			1		. EJECTOR,CKT BD:MOLD PLSTC	18677	OBD
						(ATTACHING PARTS)		
-3	214-1337-00			1		. PIN,SPRING:0.10 OD X 0.25 INCH LONG,STL	80009	214-1337-00
						- - - * - - -		
-4	136-0252-04			123		. SOCKET,PIN TERM:0.188 INCH LONG	22526	75060



READOUT INTERFACE COMPONENT LOCATION


COLUMN DATA
ROW DATA
DATA
B7 A6 B6 A5
BIT 5
BIT 6
BIT 7
BIT 8
J5
B35
B34
B33
B32
B29
A36
A33
ROW BUFFER
U40B
R53 2.2k
R90 500
ROW
R57 4.87k
VR50 7.5V
R59 2.2k
ROW & COL COM
COLUMN BUFFER
COLUMN
R73 4.87k
R91 500
R77 2.2k
U40A
VR70 12V
+15V
+50V
R79 3.9k
C70 1.0μF
ROW A-D CONVERTER
+5.1V
+15V
R51 8.2k
R60 8.2k
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
U50
COLUMN A-D CONVERTER
C10
C9
C8
C7
C6
C5
C4
C3
C2
C1
U70
ROW DECIMAL TO BINARY CONVERTER
I7 I6 I5 I4 I3 I2 I1 I0
O4 O2 O1
U61 74148
COLUMN DECIMAL TO BINARY CONVERTER
I9 I8 I7 I6 I5 I4 I3 I2 I1
O8 O4 O2 O1
ROW 2 OR 7
ROW 3
ROW 10 OR 14
U72C 7400
Q51
CR41
CR42
R40 2.4k
R42 26.1k
R44 14.0k
R46 470
R48 9.1k
-15V
U72D 7400
U65B 7486
U22A 7404
U81B 7408
U55C 7400
U65 748
U23 740
R14
74157 U62
I0a I0b I0c I0d
I1a I1b I1c I1d
S
U63 74157
ROM INPUT SELECTO
TIMESLOT 1 74147
U71
7402 U83D
U73A 7400
TS-A
TS-B
TS-C
TS-D
10B
U81C 7408
U83C 7402
TIMESLOT 1+2+3
U81A 7408
7400 U73C
7400 U72B
7408
U81D
U82D 7400
U72A 7400
COLUMN FORCE MULTIPLEXER
DISPLAY SKIP
COLUMN FORCE LOGIC
Q50
R65 470
CR65
R63 100
R62 2.2k
R64 9.1k
Q01
READOUT TRIGGER
TIMING CIRCUITRY
R83 10K
C83 .005
R67 9.1k
7400 U73D
DISPLAY SKIP
CLOCK
R81 10K
C81 270
74175 U64A
74175 U64B
U85A 74123
U85B 74123
U93B 7474
U65C 7486
U83A 7402
U64C 74175
74175 U64D
1.2μS CLOCK
C85 .001
R85 220
PLUG-INS
7438 U01D
R10 1K
U82A 7400
RESET TIMESLOT COUNTER
TRIGGER
DISPLAY TIME
STROBE
BIT 7·BIT 8
BIT 5 BUF'D
BIT 6 BUF'D

P7001

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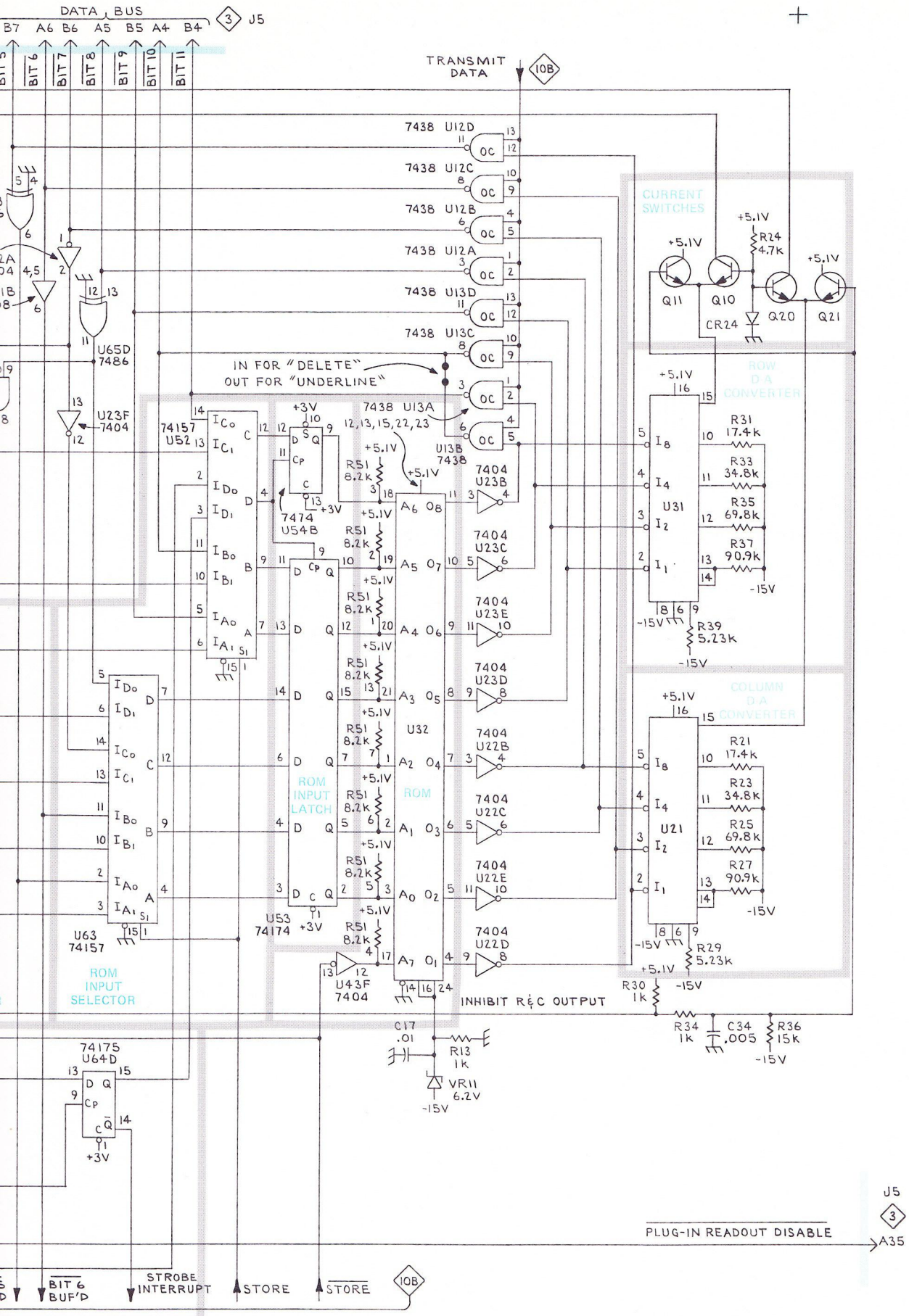

READOUT DATA CODING 10A

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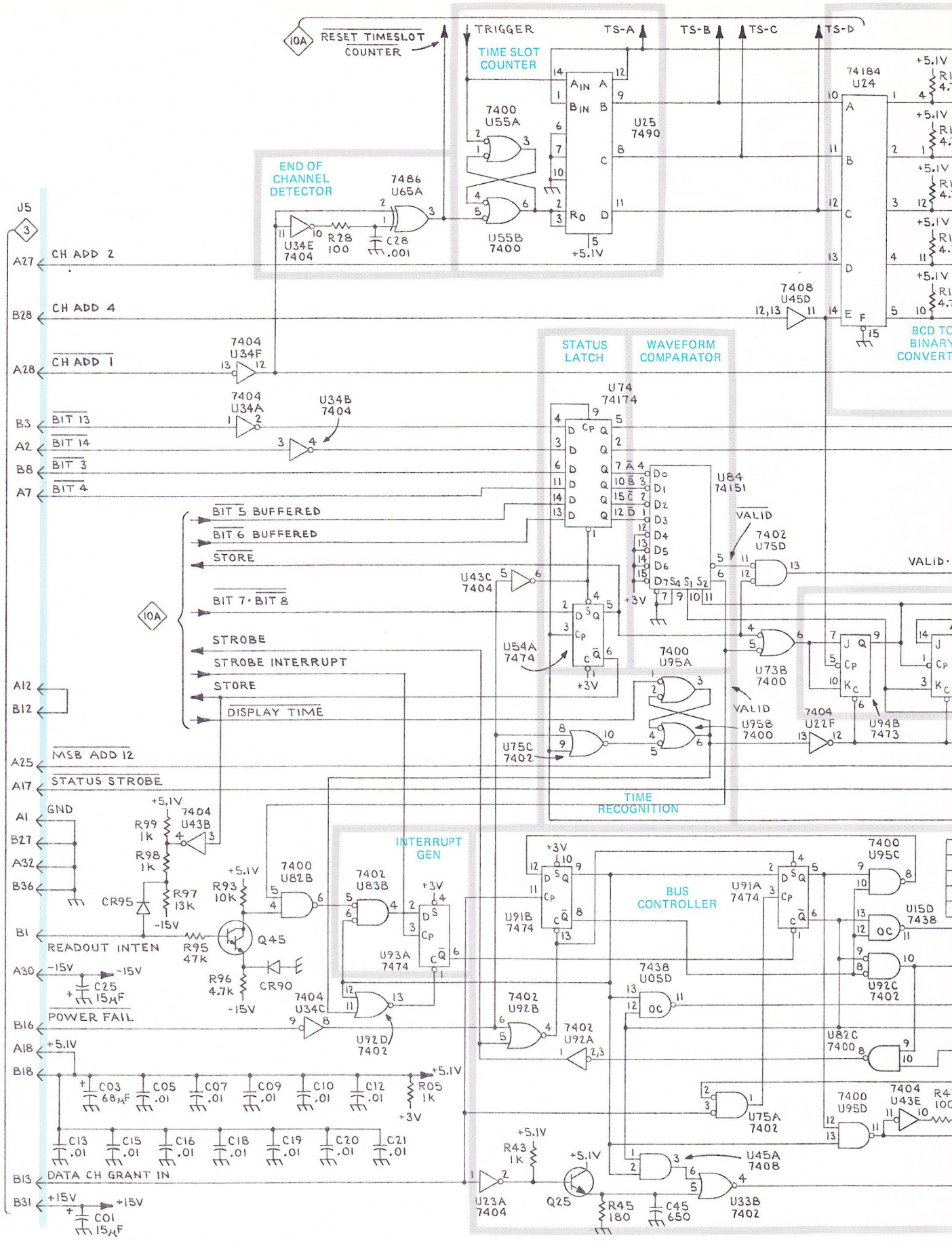
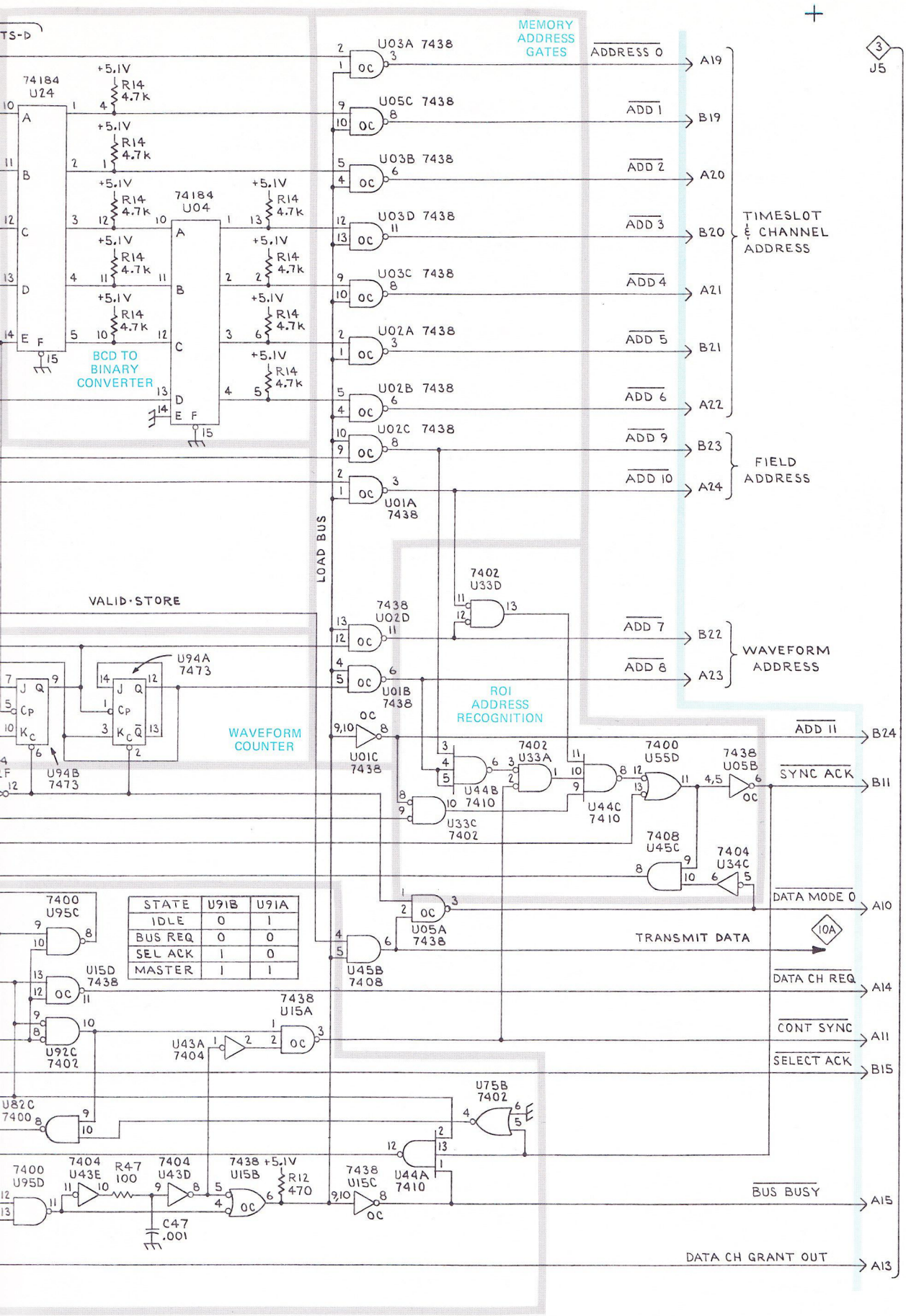

10A RESET TIMESLOT COUNTER
TRIGGER
TS-A
TS-B
TS-C
TS-D
TIME SLOT COUNTER
7400 U55A
U55B 7400
U25 7490
+5.1V
END OF CHANNEL DETECTOR
7486 U65A
U34E 7404
R28 100
C28 .001
74184 U24
BCD TO BINARY CONVERT
7408 U45D
J5
3
A27 CH ADD 2
B28 CH ADD 4
A28 CH ADD 1
7404 U34F
7404 U34A
U34B 7404
STATUS LATCH
WAVEFORM COMPARATOR
U74 74174
B3 BIT 13
A2 BIT 14
B8 BIT 3
A7 BIT 4
U84 74151
VALID
7402 U75D
BIT 5 BUFFERED
BIT 6 BUFFERED
STORE
BIT 7 · BIT 8
STROBE
STROBE INTERRUPT
STORE
DISPLAY TIME
10A
U43C 7404
U54A 7474
+3V
U73B 7400
7400 U95A
U95B 7400
U75C 7402
7404 U22F
U94B 7473
A12
B12
A25 MSB ADD 12
A17 STATUS STROBE
TIME RECOGNITION
A1 GND
B27
A32
B36
B1 READOUT INTEN
A30 -15V
B16 POWER FAIL
A18 +5.1V
B18
B13 DATA CH GRANT IN
B31 +15V
R99 1k
R98 1k
CR95
R97 13K
-15V
R95 47K
Q45
R96 4.7k
CR90
C25 15μF
7404 U43B
+5.1V
R93 10K
7400 U82B
INTERRUPT GEN
7402 U83B
U93A 7474
7404 U34C
U92D 7402
C03 68μF
C05 .01
C07 .01
C09 .01
C10 .01
C12 .01
R05 1k
C13 .01
C15 .01
C16 .01
C18 .01
C19 .01
C20 .01
C21 .01
C01 15μF
BUS CONTROLLER
U91A 7474
U91B 7474
7400 U95C
U15D 7438
7438 U05D
7402 U92B
7402 U92A
U92C 7402
U82C 7400
U75A 7402
7400 U95D
7404 U43E
U45A 7408
U33B 7402
U23A 7404
R43 1k
Q25
R45 180
C45 650
P7001
RICB
A


MEMORY ADDRESS GATES
74184 U24
74184 U04
BCD TO BINARY CONVERTER
+5.1V
R14 4.7k
U03A 7438
U05C 7438
U03B 7438
U03D 7438
U03C 7438
U02A 7438
U02B 7438
U02C 7438
U01A 7438
ADDRESS 0
ADD 1
ADD 2
ADD 3
ADD 4
ADD 5
ADD 6
ADD 9
ADD 10
A19
B19
A20
B20
A21
B21
A22
B23
A24
TIMESLOT & CHANNEL ADDRESS
FIELD ADDRESS
J5
LOAD BUS
VALID·STORE
7402 U33D
7438 U02D
U01B 7438
ADD 7
ADD 8
B22
A23
WAVEFORM ADDRESS
U94A 7473
U94B 7473
WAVEFORM COUNTER
ROI ADDRESS RECOGNITION
U01C 7438
7402 U33A
U44B 7410
U33C 7402
7400 U55D
U44C 7410
7438 U05B
ADD 11
SYNC ACK
B24
B11
7408 U45C
7404 U34C
DATA MODE 0
A10
U05A 7438
U45B 7408
TRANSMIT DATA
10A
DATA CH REQ
A14
CONT SYNC
A11
SELECT ACK
B15
7400 U95C
U15D 7438
7438 U15A
U92C 7402
U43A 7404
U82C 7400
U75B 7402
7400 U95D
7404 U43E
R47 100
7404 U43D
7438 U15B
R12 470
C47 .001
7438 U15C
U44A 7410
BUS BUSY
A15
DATA CH GRANT OUT
A13
STATE | U91B | U91A
IDLE | 0 | 1
BUS REQ | 0 | 0
SEL ACK | 1 | 0
MASTER | 1 | 1

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Change Reference: M34035 Date: 6-6-79

Product: P7001 READOUT INTERFACE (670-2385-00) 070-1609-00 EFF SN B100681

CHANGE	DESCRIPTION

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES

CHANGE TO:

	670-2385-01	CKT BOARD ASSY:READOUT
U01	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U02	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U03	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U05	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U12	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U13	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U15	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U54	156-0041-05	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP
U55	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
U72	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
U73	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
U82	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
U91	156-0041-05	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP
U93	156-0041-05	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP
U95	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
ADD:	(DIAGRAM 	READOUT DATA CODING)
R26	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W
R38	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W
R52	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W
R61	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W

R26 is added from pin 8 of U21 to -15 V. R38 is added from pin 8 of U31 to -15 V.

R52 is added from pin 8 of U50 to +15 V. R61 is added from pin 8 of U70 to +15 V.